

Product Overview

- Reads Verilog RTL or gate-level design (pre-JTAG) & generates a BSDL file
- Synthesizes JTAG from BSDL and inserts results into design
- Modifies pad instantiations to implement boundary scan registers
- Adds instantiations to implement other JTAG functions
- Includes library of synthesizable Verilog JTAG logic for JTAG functions
- Complements SAJE JTV's BSDL file-driven technology
- Generates correct-on-first-pass JTAG design

Product Description

SAJE JTS has been developed by SiliconAid Solutions to provide a low-cost production ready IEEE Std. 1149.1 and 1149.6 boundary scan implementation. The tool utilizes a BSDL-centric approach that supports Verilog synthesizable design flows. SAJE JTS represents a cost effective means to develop and implement IC product specific DFT strategies when used in conjunction with today's complex-fault modeling ATPG tools and the SAJE JTV JTAG verification tool.

JTAG is a BSDL-centric board-test approach. For a device to be JTAG compliant, an associated verified BSDL file must be provided to drive the board-level automatic test pattern generator. Therefore, the problem from the semiconductor manufacturer product perspective is to create a verified JTAG-compliant device, an associated verified BSDL file, and production test patterns.

For design scenarios with no BSDL starting-point file, SAJE JTS can read a Verilog design prior to JTAG insertion and automatically generate a BSDL file. Generation is per pre-defined tool defaults supplemented with user-defined commands. Public instructions are supported but some instructions require additional customized design. User instructions, Runbist, and analog test receivers require additional design for test development that may be addressed with SiliconAid consulting assistance as required.

Using the BSDL file, the SiliconAid SAJE JTV tool can generate a custom testbench and a suite of test patterns to verify design functionality using Verilog simulation. SAJE JTS provides a testbench customization file to facilitate the SAJE JTV tool's ability to verify many internal JTAG design nodes as well as external pins. Successful verification includes both the JTAG Verilog design and the associated BSDL file.

The SAJE JTV tool can also provide chip manufacturing production test patterns. The SAJE JTS and JTV tools provide the chip designer with a complete solution for designing JTAG,

verifying JTAG design and BSDL correctness, and generating test patterns for production tester.

SAJE JTS Features

- Generates synthesizable Verilog JTAG design defined by BSDL file
- BSDL file can be learned from non-JTAG Verilog design
- Verilog can be RTL or gate-level statements
- Generates IEEE 1149.1 compliant boundary scan logic
 - Supports IEEE Std. 1149.1-2001 Standards
 - Supports all public instructions
 - Intest and Runbist require additional design
- Generates library of JTAG functions
 - Includes synthesizable Verilog RTL for JTAG functionality
 - Includes non-synthesizable version of analog test receiver for digital simulation
- Flip-flop-based design, gated or non-gated clocking styles
- User friendly graphical-user-interface(GUI)
- Interactive or command-line control from Dofile
- Generates a testbench customization file for the SAJE JTV verification tool

SAJE JTS Universal Design-Flow Fit Diagram

