

JTV™ 4.3.4 Product Overview

- Used successfully on hundreds of production IC tape-outs
- Ensures correct JTAG functionality on first-pass silicon
- Verifies that the BSDL file matches the JTAG design
- Generates STIL-formatted functional and parametric production tests
- Helps find fab-related pad logic yield problems
- Supports verification of both 1149.1 and 1149.6 designs
- Includes support for user-defined tests
- Both Linux and Solaris platforms are supported

JTV™ Product Description

SAJE JTV was developed over a ten-year period by JTAG practitioners at Freescale Semiconductor (formerly Motorola SPS) and significantly enhanced by SiliconAid Solutions over the last six years. JTV is protected with a US Patent.

The tool uses a BSDL-driven approach and is well suited for design flows in which the JTAG design is derived from earlier designs or synthesized from third-party tools. JTV serves as an independent verification tool to lower the risk of design-related defects.

BSDL (Boundary Scan Description Language) describes the JTAG implementation for a particular device. SAJE JTV includes an interactive BSDL editor based on a GUI-driven approach that can be used to create a BSDL file.

SAJE JTV provides a large robust suite of automatically generated tests to verify a JTAG implementation and the associated BSDL file. During the design phase, these tests support comprehensive design verification while eliminating the need to manually write unit tests or a verification testbench.

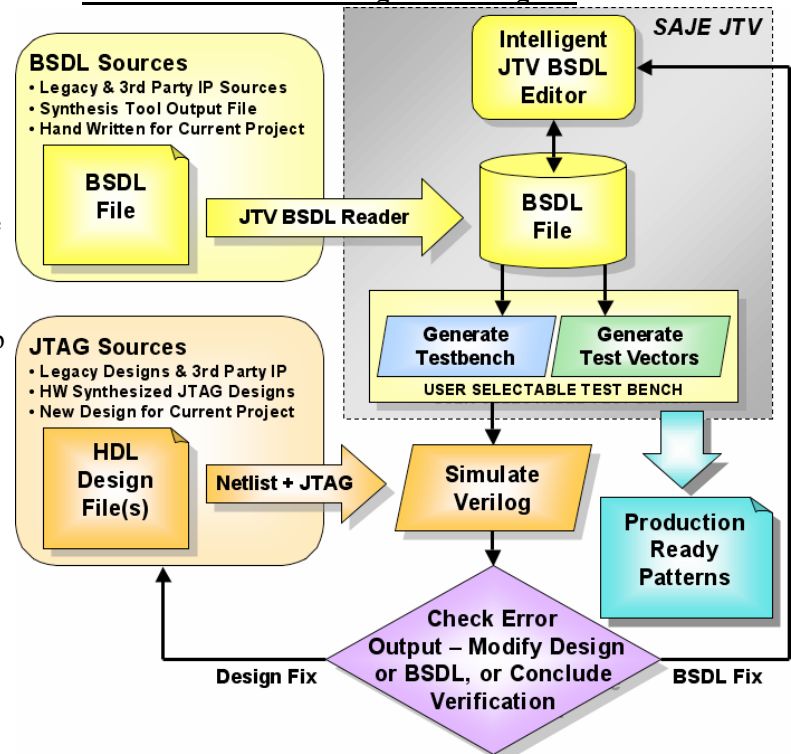
For silicon debug, JTV automatically generates high-quality production ready test patterns that facilitate first-silicon bring-up on debug stations or automatic test equipment (ATE). During manufacturing, the tests provide high-quality data to drive yield analysis processes.

The test suite includes 40 individual test procedures, 12 optional internal JTAG-related test points, 10 implementation options, and 14 output options. The tests are ordered from low to high complexity. The first simple tests provide data flushing while advanced complex tests fully verify the JTAG implementation against the requirements of the 1149.1 and 1149.6 standards. Both fault-simulated production test patterns and parametric tests are provided that can be either simulated or converted directly to STIL formatted output.

SAJE JTV™ Major Features

- Supports many design styles including gated and non-gated clock design and master-slave flip-flops
- Generates a verification testbench from a BSDL file with means to fully customize it with a user-generated script
- Test and testbench generators can be invoked by scripts or interactively from the command line or GUI.
- Generates commented simulation output to reduce debugging effort
- Provides a self-checking environment that includes response prediction of internal JTAG test points for earlier detection and diagnosis of problems
- Generates STIL formatted patterns for ATE
- Provides optional parallel-load format (no shifting) to reduce simulation times for lengthy tests with large designs
- Supports IEEE Std. 1149.1-1993, Std. 1149.1-2001, and 1149.6-2003
- Provides verification support for SAMPLE capture functionality and RUNBIST instruction
- Provides a user-defined test capability using either SVF or JTV's binary-based language .

SAJE JTV Universal Design-Flow Diagram





SAJE™ JTV – JTAG and BSDL Verification and Debug

The SAJE JTV startup screen is shown in **Diagram 1** at right. The three large button choices invoke the BSDL editor, the JTAG ATPG and, Testbench modules, respectively. The blue “Std_1149_6 Options” button enables verification of IEEE Std. 1149.6 design features.

The BSDL editor facilitates the creation of a new BSDL file or the modification of an existing BSDL file. The BSDL editor startup screen is shown in **Diagram 2**.

The ATPG Test Select screen is shown in **Diagram 3** and is used to select one or more tests from the 40 built-in JTAG tests. Tests are ordered from simplest to most complex to facilitate design verification and silicon debug. The ATPG Test Options screen is shown in **Diagram 4** and is used to enable ATPG prediction for internal nodes, design implementation options, and output options. The blue labels indicate IEEE Std. 1149.6-related verification tests and options.

The Testbench screen is pictured in **Diagram 5** and provides control over generation of a Verilog-compatible testbench. The screen enables the user to control related input/output files, and configuration control over the internal JTAG state and implementation options.

SAJE JTV offers the ability to verify and test robust JTAG product test features in complex IC designs. Additionally, it supports the creation and validation of proven accurate BSDL files which is a critically important deliverable. SAJE JTV is unique in its ability to verify that the chip design is JTAG-compliant and that the BSDL file accurately describes the JTAG design.

Diagram 1 –Startup Screen

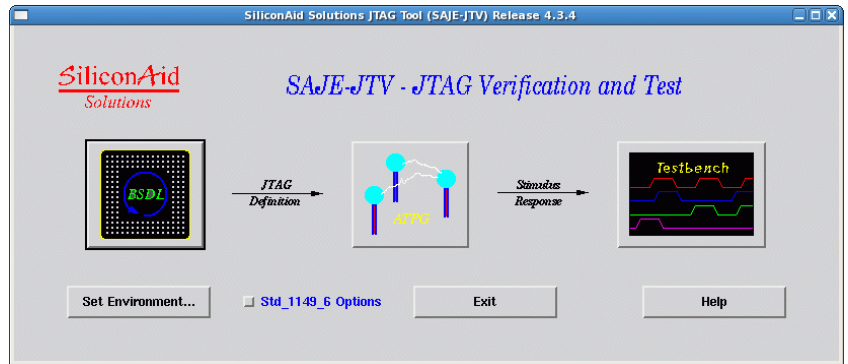


Diagram 2 – BSDL Editor Screen

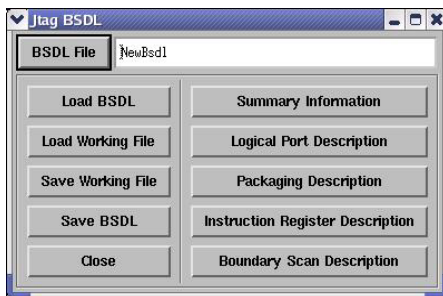


Diagram 3 – ATPG Test Select Screen

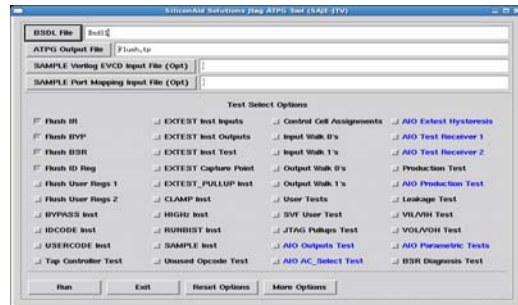


Diagram 4 – ATPG Test Options Screen

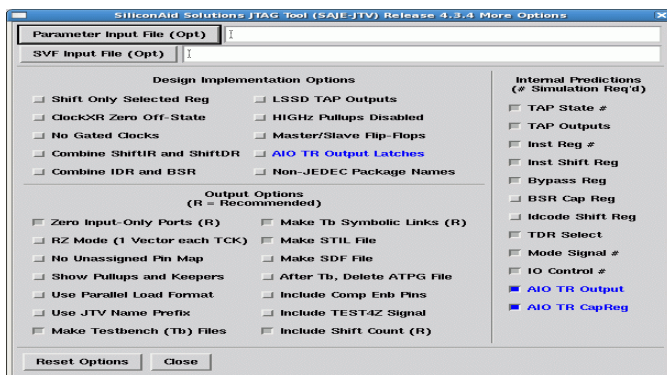


Diagram 5 – Testbench Screen

