Scan Compression with Magma Talus Design

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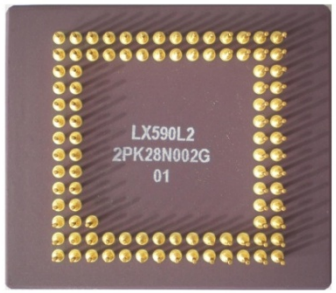
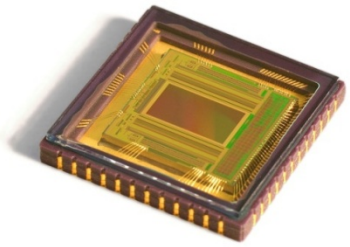
Introduction

- **Welcome**
- **AltaSens Team:**
  - **Debo Sekoni**, Sr. Design Engineer – DFT
  - **Lygia Ionnitiu**, Technical Documentation Manager

About AltaSens



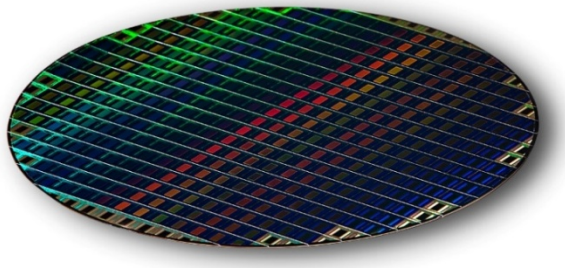


Videoconferencing

- **AltaSens is the premier supplier of high-performance CMOS image sensors for high definition (HD) video.**

Security

Broadcast & Cinematography



The Problem

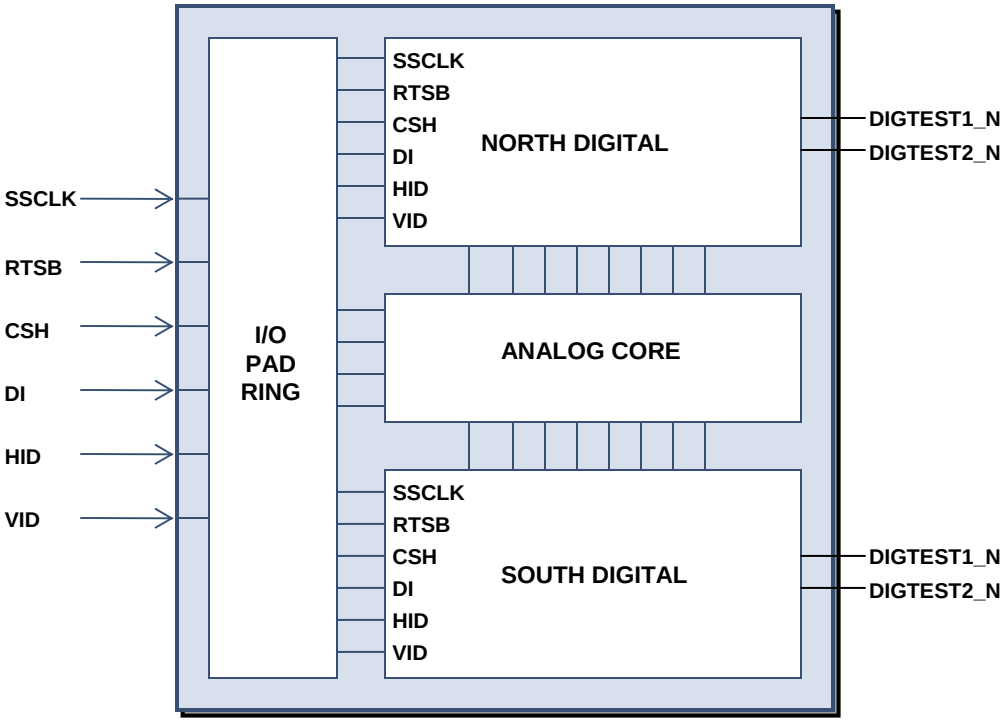
- Our design was pin-limited and required scan compression.
- We wanted to stay with Talus.
- Talus did not support scan compression.
- We needed a solution.

The Solution

- **Achieving a compression ratio of 100x by using a three-step process to integrate Magma Talus Design with Mentor Graphics Tessent TestKompress:**
  1. Inserting Scan Logic for Compression
  2. Inserting Scan Compression
  3. Running ATPG for Scan Compression

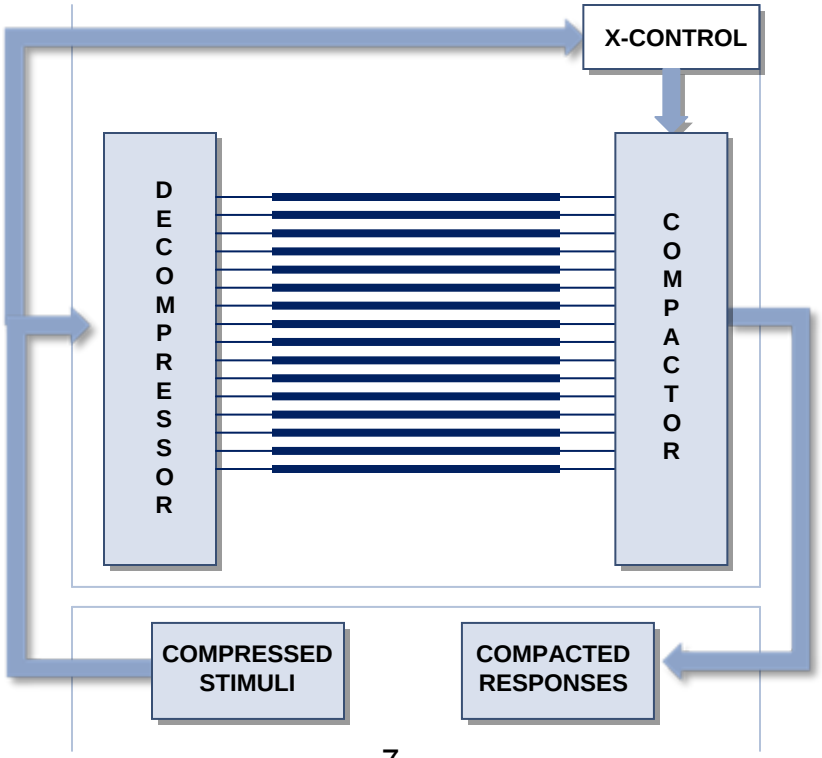
The Design

- **Mixed-signal System on Chip (SoC)**



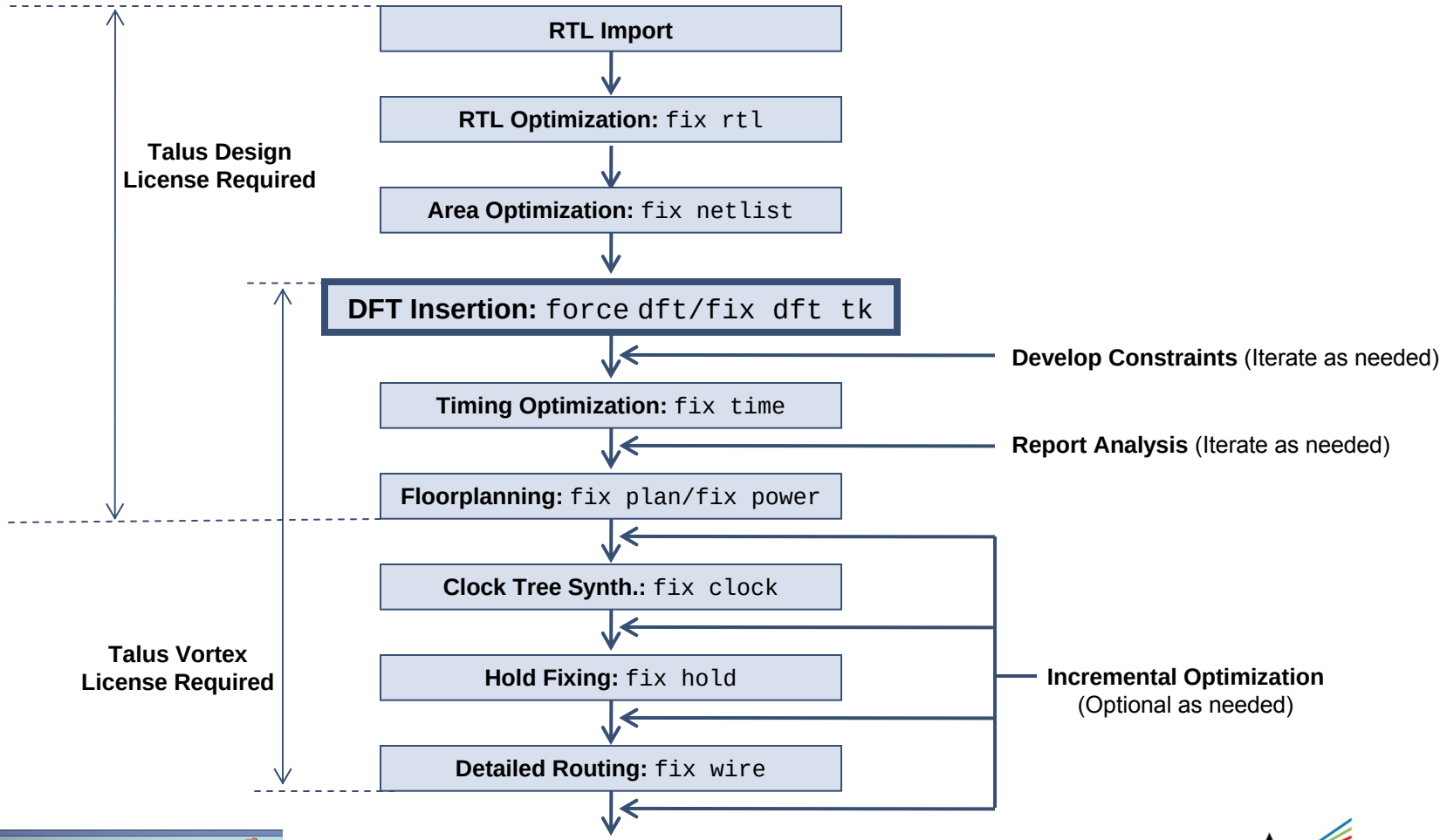
The DFT Tools

- **Magma Talus Design**
  - Top-down Flat flow (default)
- **Mentor Graphics Tessent TestKompress**
  - What is Embedded Deterministic Test (EDT)?

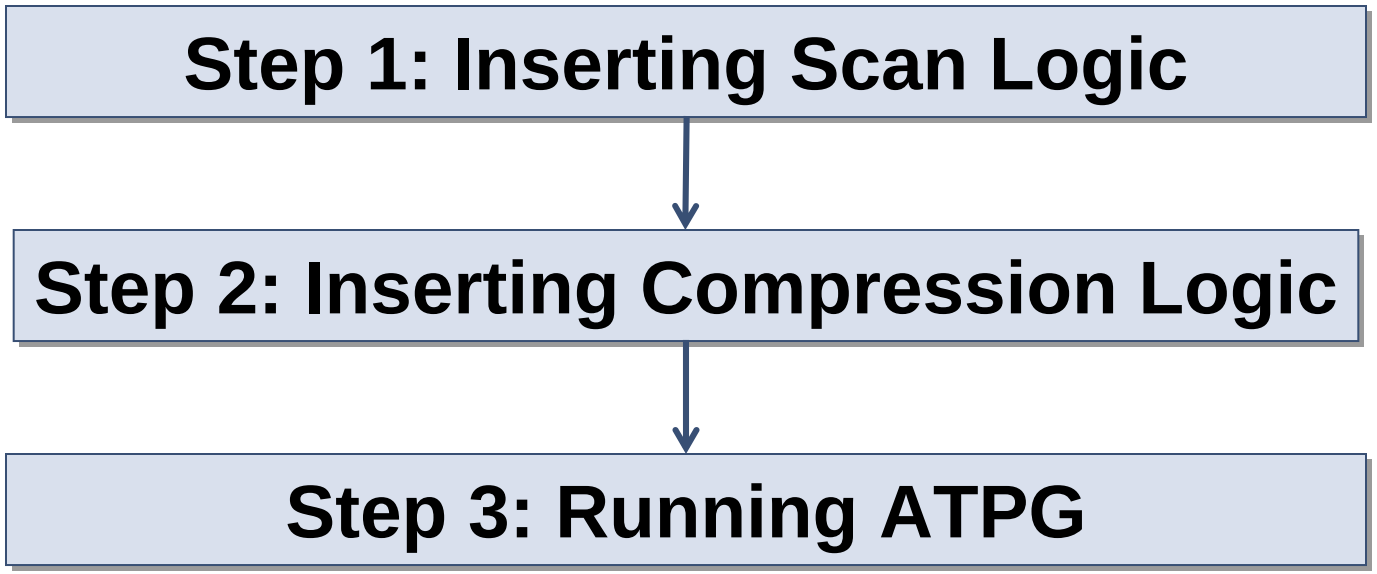


Methodology Overview

- **Talus Compression Design Flat Flow:**

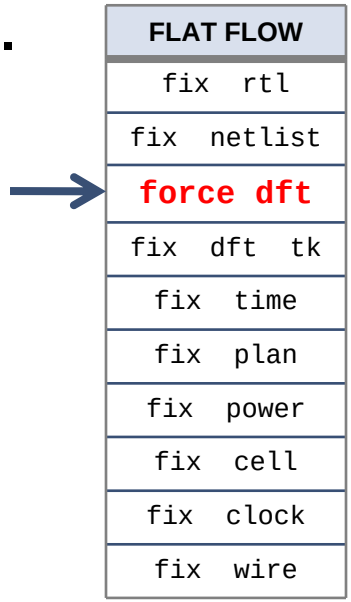


Methodology



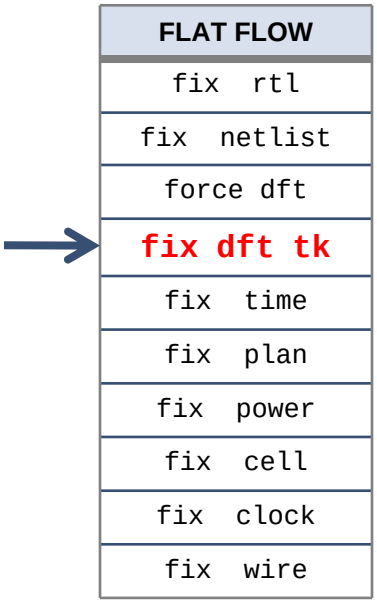
Step 1: Inserting Scan Logic

- Define I/O pins for scan compression DFT architecture.
- Configure I/O pins for scan compression DFT architecture.
- Define scan chains for scan compression DFT architecture.
- Define flip-flops to be excluded from scan logic insertion.
- Identify automatic DFT repair functions to enable by running pre-scan DFT design rule checks (DRC).
- Enable automatic DFT repair functions.
- Configure scan chain mixing.
- Re-run pre-scan DFT DRC.
- Insert scan logic for scan compression.
- Run post-scan DFT DRC.
- Review pre-scan and post-scan DFT DRCs.



Step 2: Inserting Compression Logic

- Call the third-party test compression tool, Mentor Graphics Tessent TestKompress.
- Generate the EDT logic.
- Synthesize the EDT logic.
- Connect the scan chains to the EDT logic.
- Connect the scan channels to the EDT logic.
- Integrate the EDT logic into the top-level.



Step 3: Running ATPG

- Edit the *mydesign*_blk_atpg.edt.do file
- Edit the run_atpg_edt_blk_*mydesign*.csh file
- Run ATPG
- Review ATPG results

Non-Compression vs Compression Results

Scan Test Statistics	NON-COMPRESSION DIG_TOP	COMPRESSION DIG_TOP
Test Coverage:	92.03%	92.76%
ATPG Effectiveness:	99.82%	99.82%
No. of Chain Test Patterns:	1	136
No. of Transition Scan Test Patterns:	19,663	21,852
No. of Stuck-@ Scan Test Patterns:	2,923	3,987
Total Pattern Count:	22,587	25,975
Volume of Chain Test Patterns:	109,600	102,768
Volume of Transition Scan Test Patterns	2,155,064,800	19,404,576
Volume of Stuck-@ Scan Test Patterns:	320,360,800	3,540,456
Total Scan Test Pattern Volume:	**2.48 Gb (2476 Mb)**	**0.023 Gb (23 Mb)**
ATE Test Time		
No. of Scan Cells:	109,600	109,318
No. of Scan Chains:	4	200
No. of Scan Patterns	22,587	25,975
Frequency:	20 MHz	20 MHz
No. of Tester Cycles:	618,883,800	14,197,675
Tester Time (seconds):	**30.94**	**0.71**

Results Calculation Methods

$$\text{Number of test cycles} = \frac{\text{Number of scan cells}}{\text{Number of scan chains}} \times \text{Number of scan patterns}$$

$$\text{Test time (seconds)} = \text{Number of test cycles} \times \frac{1}{\text{Frequency (MHz)}}$$

$$\text{Test cost (\$\$\$)} = \text{\$ 0.xx per second}$$

The Benefits

- **What we gained from the integration of Magma Talus Design with Mentor Graphics Tessent TestKompress?**
  - Stayed within Talus to maintain design methodology from RTL to GDSII.
  - Provided high-quality test vectors for pin-limited designs with only 8 digital I/O pins or less.
  - Reduced prohibitive costs of high-end ATE by keeping test data volume and application time to a minimum.
  - Minimized test interface requirements during wafer test.
  - Took advantage of cheaper ATE that do not support large number of I/O pins.

Lessons Learned

- **Learning curve**
  - Give yourself enough time
  - Familiarize yourself with the Application Documentation to help reduce frustration
  - Learn the Tool Command Language (TCL)

- **Advantages of teaming up with Magma & Mentor Graphics R&D**
  - Pranay Prakash, Director (R&D)
  - Bill Keller, Application Engineering Consultant