

An Introduction to IEEE P1149.7

IEEE P1149.7:
a complementary superset of the
IEEE 1149.1 standard

Agenda

◆ History:

- Standards vs. Proprietary solutions

◆ Benefits:

- Compatibility with existing technology and tools
- Reducing the number of pins
- New connection topologies
- Gateway for advanced technology and instrumentation

◆ Summary

Vote: How many people here use:

A) JTAG for Boundary scan?

B) JTAG for debugging?

C) JTAG for Design Verification?

C) ?

What is IEEE P1149.7?

- ◆ What is IEEE 1149.1 (JTAG)?
 - Connection for manufacturing test (BSDL)
 - Connection for debugging software

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- ◆ What is IEEE P1149.7?
 - A new IEEE standard currently in process
 - P1149.7 is **not** a replacement for 1149.1
 - P1149.7 uses 1149.1 as its foundation
 - P1149.7 provides 1149.1 extensions
 - P1149.7 provides 2-pin operating modes
 - P1149.7 provides a standard gateway to the pins

P1149.7 History and Status

● **MIPI Origins**

- Objective – define a backwards compatible minimum pin debug interface
- Strategy – requirements gathering, technical debate
- Tactics – solicit competing proposals, choose a winner
- **Result – P1149.7 was handily selected as winning proposal vs. SWD**

◆ **Collaboration with Nexus consortium**

- Objective – Compare common needs, explore common solution
- Strategy - Joint meetings, compare requirements
- Tactics - Specifications reviewed, incorporate feedback
- **Result – Agreement to pursue IEEE standard because of large field of use**

◆ **IEEE PAR approved**


- Test, Debug, and backwards IEEE 1149.1 compatibility considerations
- Specification reviewed, balloting closed.
- **Presumed Result – IEEE 1149.7 standard in 2Q09**

◆ **Implementation Ready**

- DTS and TS IP available from **IPeXtreme**
- Verification solutions available from **Globetech**

Standards Focus

1149.1 vs. P1149.7

	1149.1	P1149.7
Test	Boundary Scan: Finding card level connectivity issues	Compliance: Preserving boundary scan for system-on-chip (SoC)
Apps		Capability: Features for debug

IEEE 1149.7 Target

Test	Compliance	<ul style="list-style-type: none">•Ensure compliance with 1149.1 to enhance compatibility with industry test infrastructure
Apps	Capability	<ul style="list-style-type: none">•Power: Test logic power-down•Performance:<ul style="list-style-type: none">•Shortened multi-chip scan chains•Glue-less Star configuration•Faster downloads to target•Equivalent performance with fewer pins•Pins: Reduce pin usage while adding functions•Instrumentation •Customization

1149.7 “Classes”

◆ IEEE 1149.1 Extensions

- ◆ Class T0 – Ensure IEEE Compliance for chips with multiple TAPs
- ◆ Class T1 – Add control functions (e.g. functional reset, power)
- ◆ Class T2 – Add performance features for Series configurations
- ◆ Class T3 – Add Star configuration

◆ Advanced Two-Pin Operation

- ◆ Class T4 – Add two pin operation
- ◆ Class T5 – Add instruction/custom pin use to two pin operation

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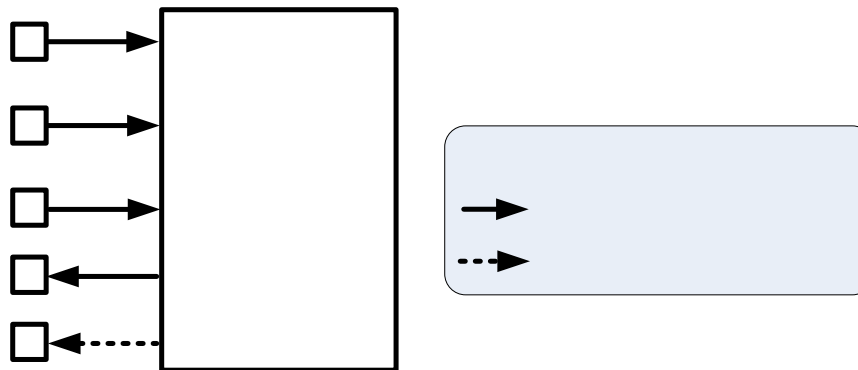
◆ Summary

Why is Compatibility Important?

- ◆ IEEE1149.1 (JTAG) is ubiquitous in industry, for both TEST and DEBUG applications.
 - Available on microcontrollers through to microprocessors
- ◆ Decrease risk and **preserve industry investments**
- ◆ **Preserve customer investments.**
- ◆ Simplify transition to advanced IEEE 1149.7 technology
- ◆ Re-use of investments in software, tools, and hardened IP

Compatibility with existing technology and tools: Class T0

- ◆ TAP behavior is IEEE 1149.1 compliant
 - N-bit IR
 - 1-bit DR for bypass instruction
 - IDCODE requirement is mandatory (32 bit path)
 - Mandatory instructions behave as specified in 1149.1 specification
- ◆ Interface behavior is compliant between:
 - Test-Logic-Reset TAP state and
 - First operation that changes the IR and DR scan path configuration to operate appear as multiple TAPs connected in Series with separate instruction register and data register scan paths (similar to a board on chip).



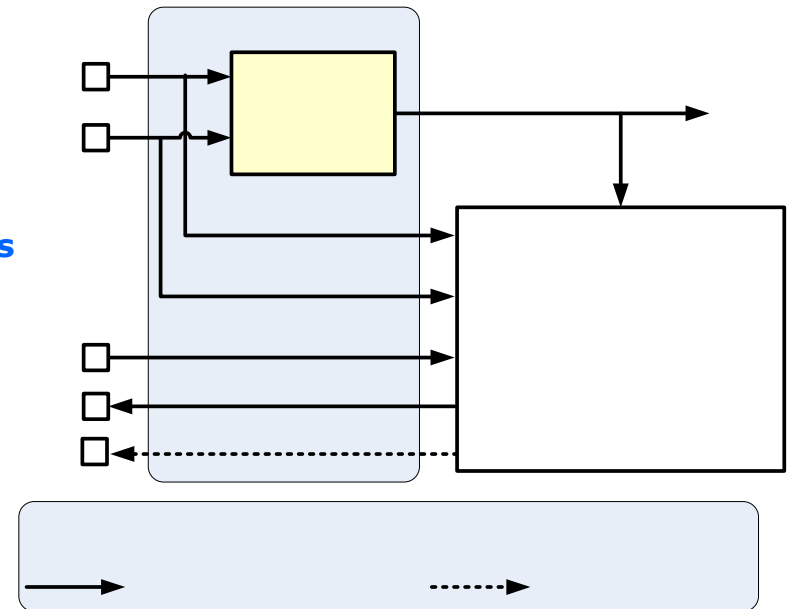
Compatibility with existing technology and tools: Class T1

- ◆ A control mechanism that is driven by TAP state sequences is added
 - Creates a second command and control mechanism
 - Transparent: does not use or change IR and DR scan path lengths
 - Novel use of tap state sequences and shift states
 - Foundation for 1149.7 Class T1 and above.
- ◆ Features
 - Test Reset – reset the STL
 - Functional reset - reset functional logic
 - Interface power management (4 modes)

Key Innovation!

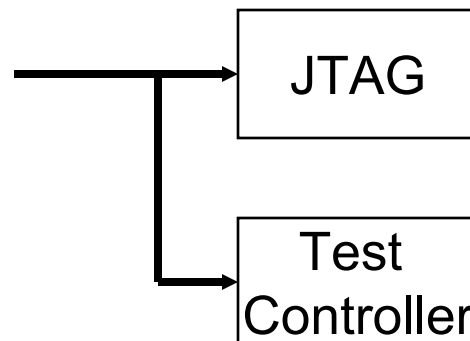
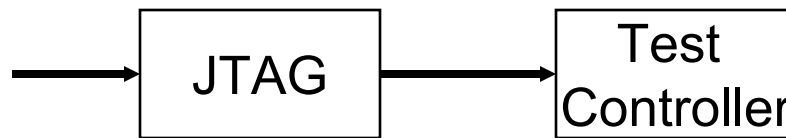
Optional Features

- Same interface as IEEE 1149.1 TAP
- Control operates in parallel with system TAP controllers



Compatibility with existing technology and tools

- ◆ Selection mechanism (Reset and Selection Unit-RSU) allows interoperability with proprietary, legacy and IEEE 1149.7 technologies.
- ◆ Unique escape sequence on TMS320 while TCK is logic 1
- ◆ Enable Inter or Intra-chip technology interoperability



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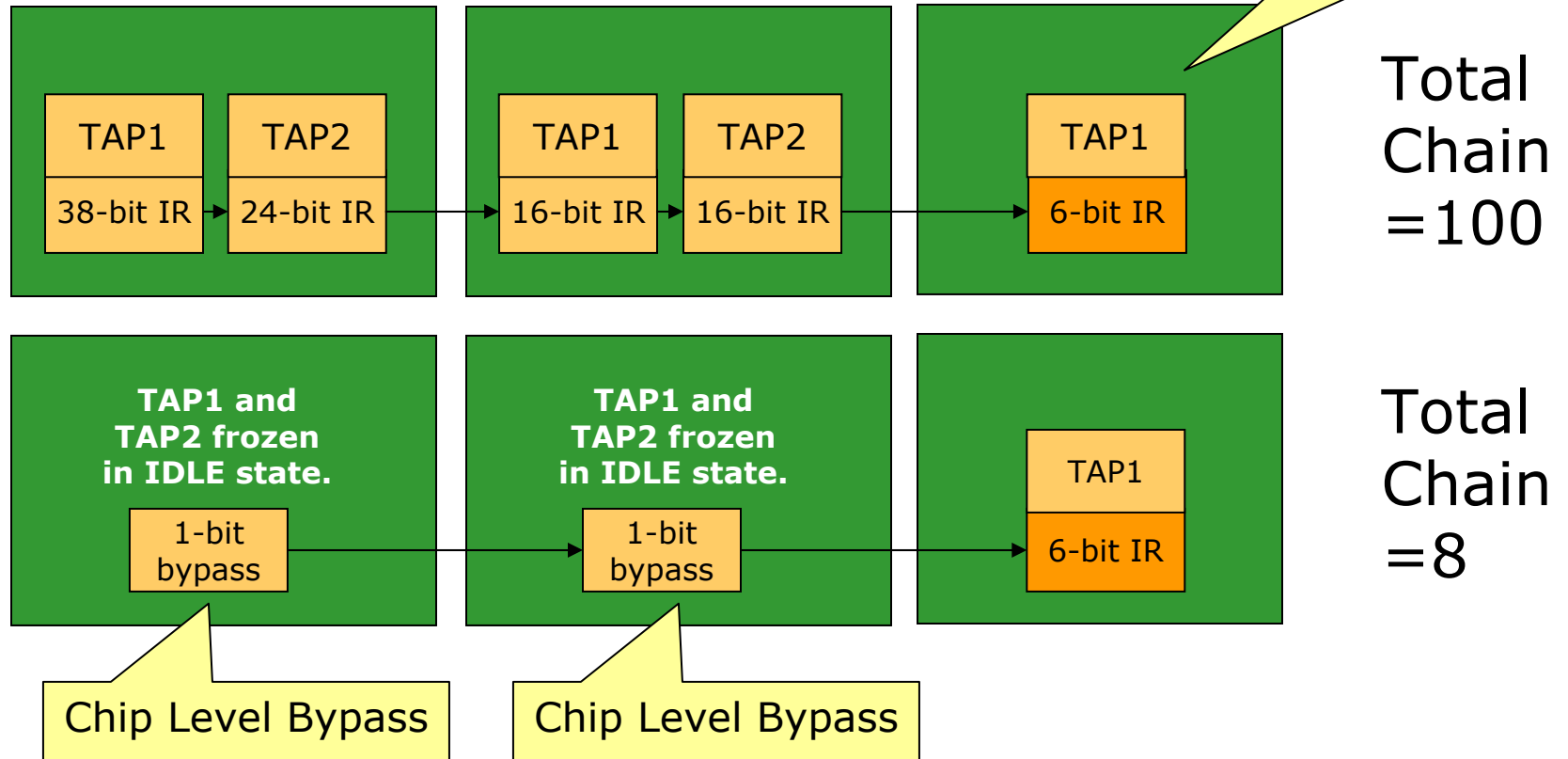
Quiz: Who has seen 20 cores in a
JTAG scan chain?

Bonus: What determines your debug performance
there?

Series Bypass

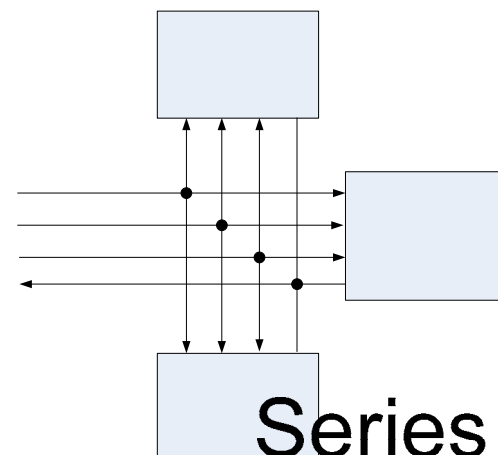
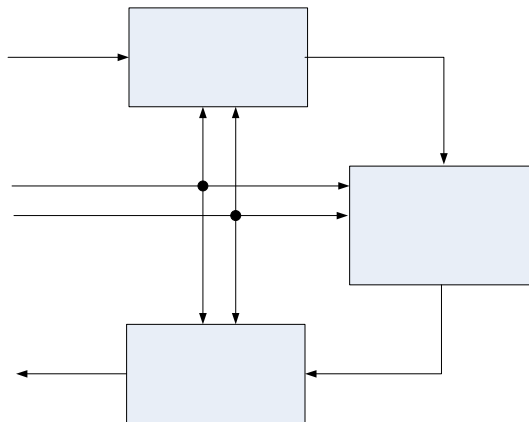
◆ Uses TAP selection and bypass bit to:

- Improve Series connected devices scan performance using 1-bit chip bypass for very long scan chains
- Create a “firewall” to protect system operation when DTC is connected or disconnected from the TS



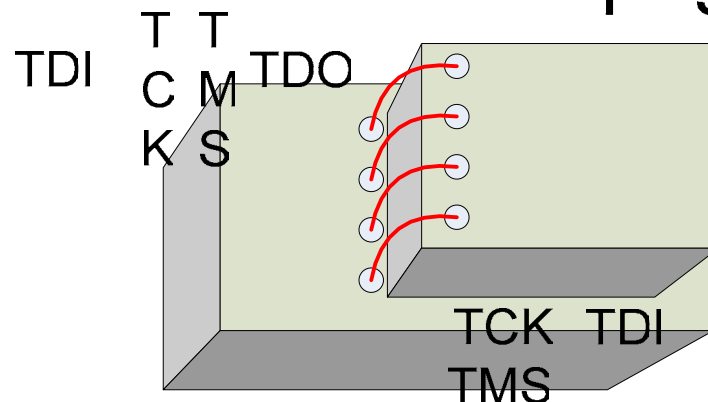
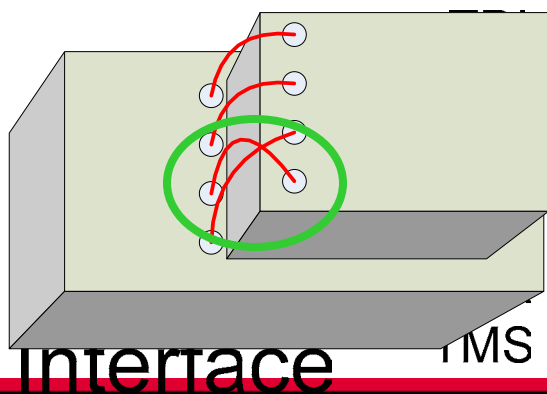
New connection topologies

- ◆ Both Series and Star topographies are supported



Series Star
Topography

- ◆ Star topology is favorable for stacked die



How does Boundary Scan work in Star configuration

- ◆ The key to using boundary scan capability afforded by IEEE1149.1 and IEEE 1532 is to have the Series and Star scan operations appear functionally equivalent.
- ◆ When in a IEEE1149.7 Star configuration, scan operations are functionally equivalent to the Series scan operations when:
 - Capture-xR and Update-xR TAPC states are synchronized among a group of selected TAP.7 controllers
 - Scan data associated with this group of TAPs is exchanged between one TAP at a time between these states.
 - ◆ TAPs need to be selected and de-selected without going the Capture-xR and Update-xR
- ◆ Thus, from a BSDL perspective, all operations appear as a Series scan.

Quiz: How much does each pins on a package cost?

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◆ History:

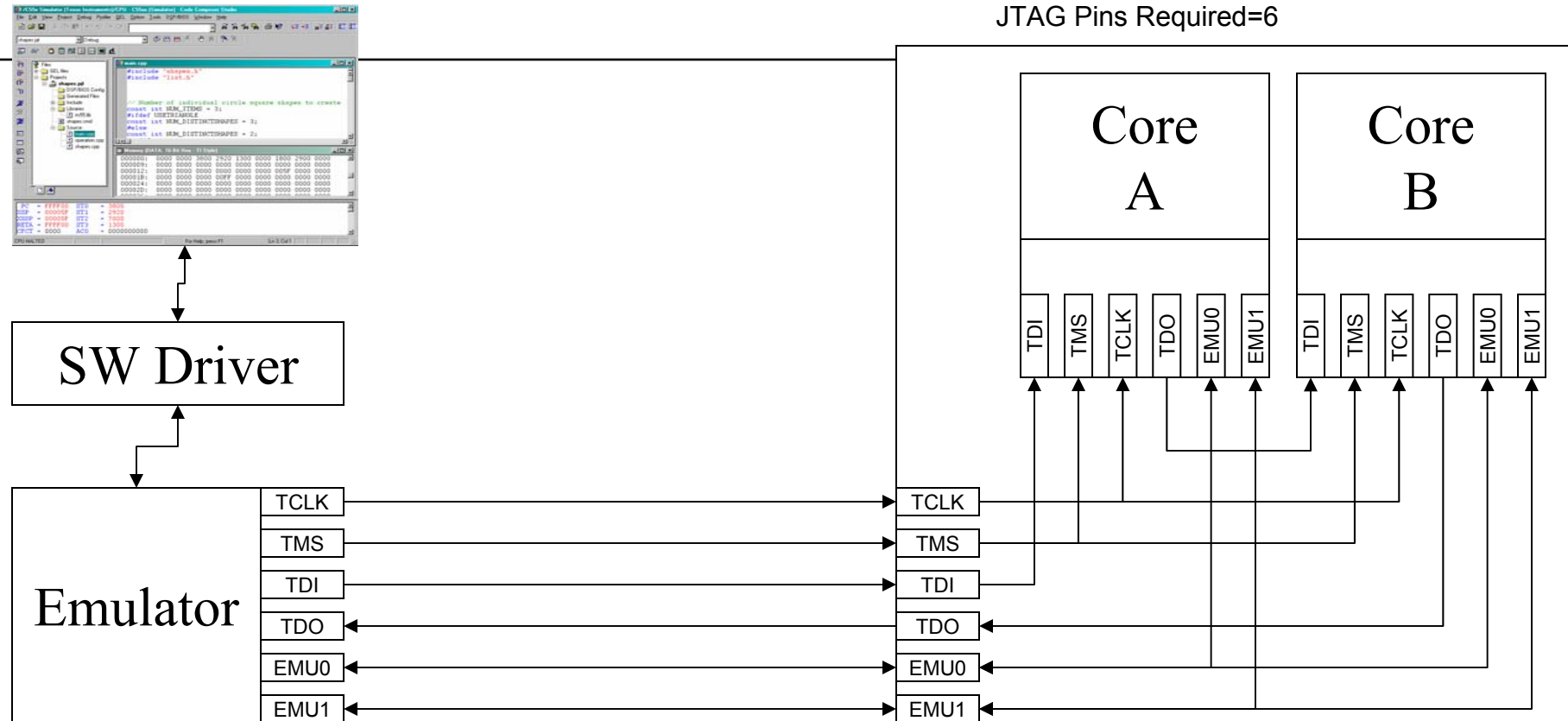
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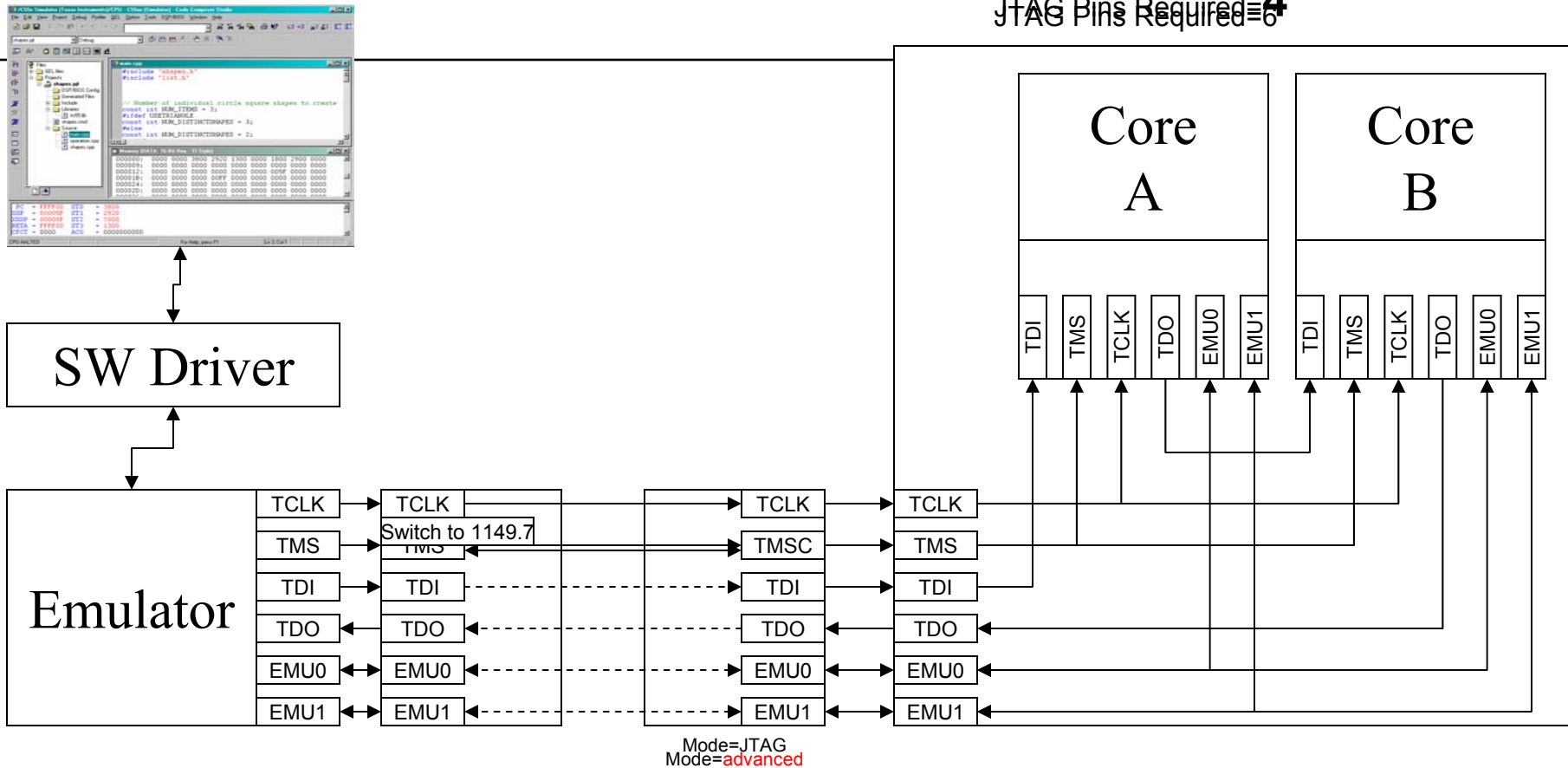
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Extending JTAG



Extending JTAG

JTAG Pins Required = 4



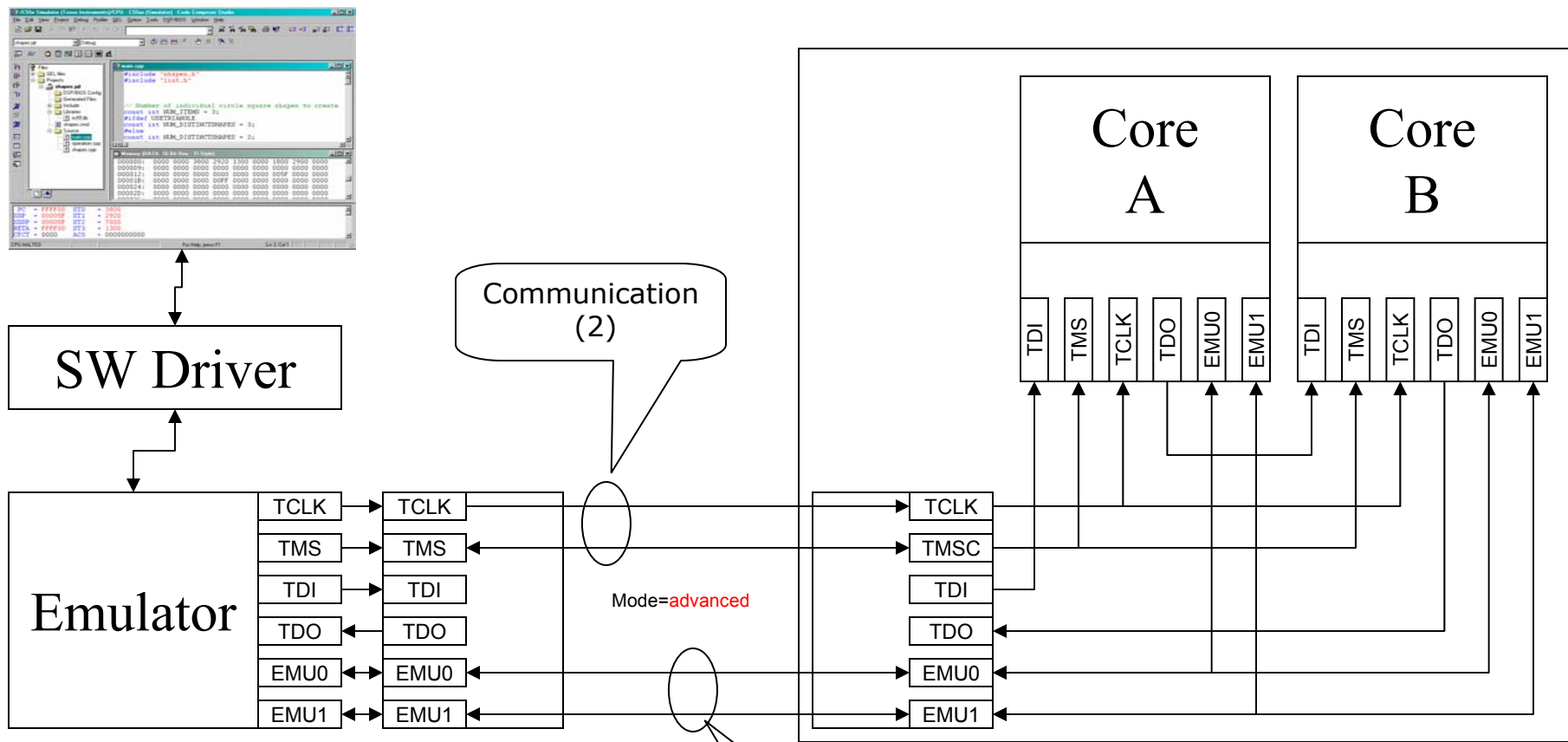
- Use adapters to prototype with existing IEEE1149.1 HW and SW
- IEEE1149.7 starts in 1149.1 mode for compatibility
- Switch the Adapter to IEEE1149.7 mode by sending a command

- TMS is now TMSC
- TDI and TDO are now optional

----- Optional signal

Communication Pin Reduction

Communication pin reduction from 4 to 2

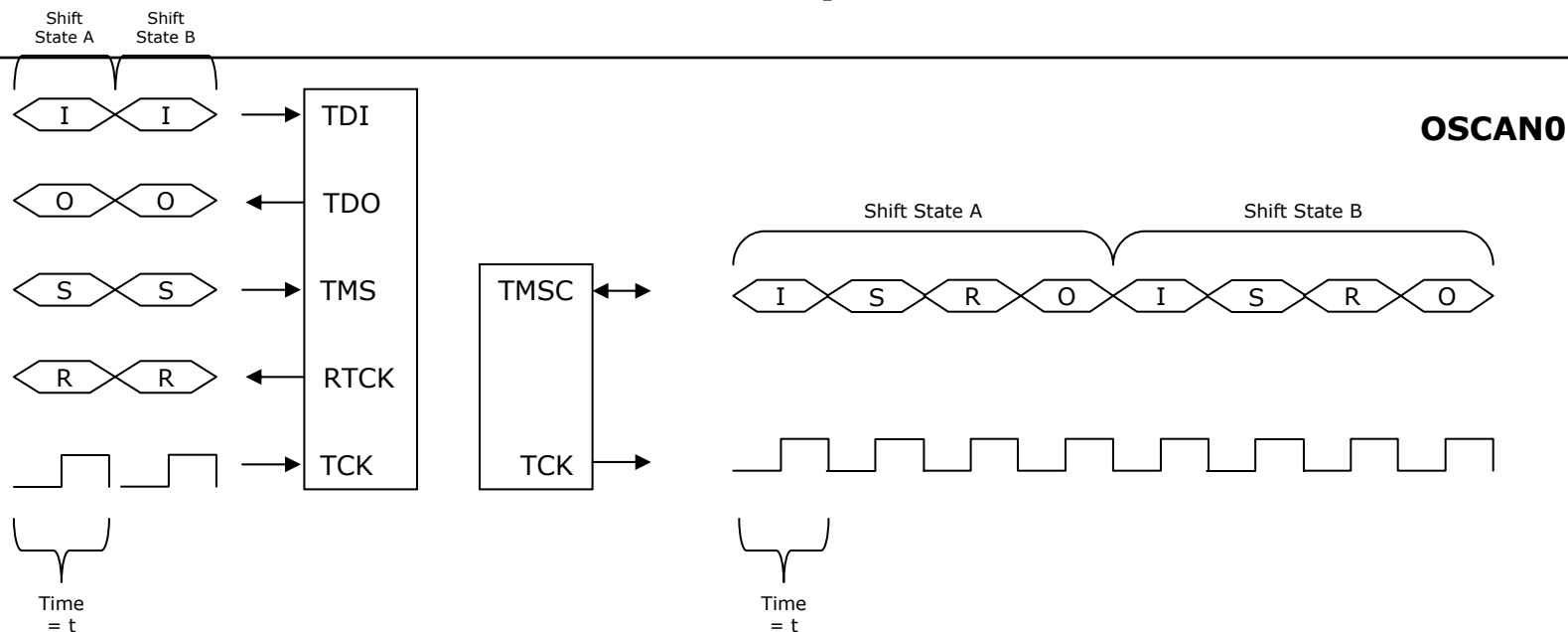


As IEEE 1149.7 only uses TAP state sequences via the TCK and TMS pin to manage the TAP controller, it is possible to start up in IEEE1149.1 protocol with 2 physical pins and change to IEEE 1149.7 advanced protocol.

Instrumentation (2)

Vote: How many people think new SoC devices are constructed from completely new cores and IP?

2 Pin Operation



- 2 Pin mode operation is essentially a parallel to serial conversion
- Different OSCAN modes apply different optimizations, increasing performance
 - Ex: Return TCLK, Download only, TCK Rate, etc

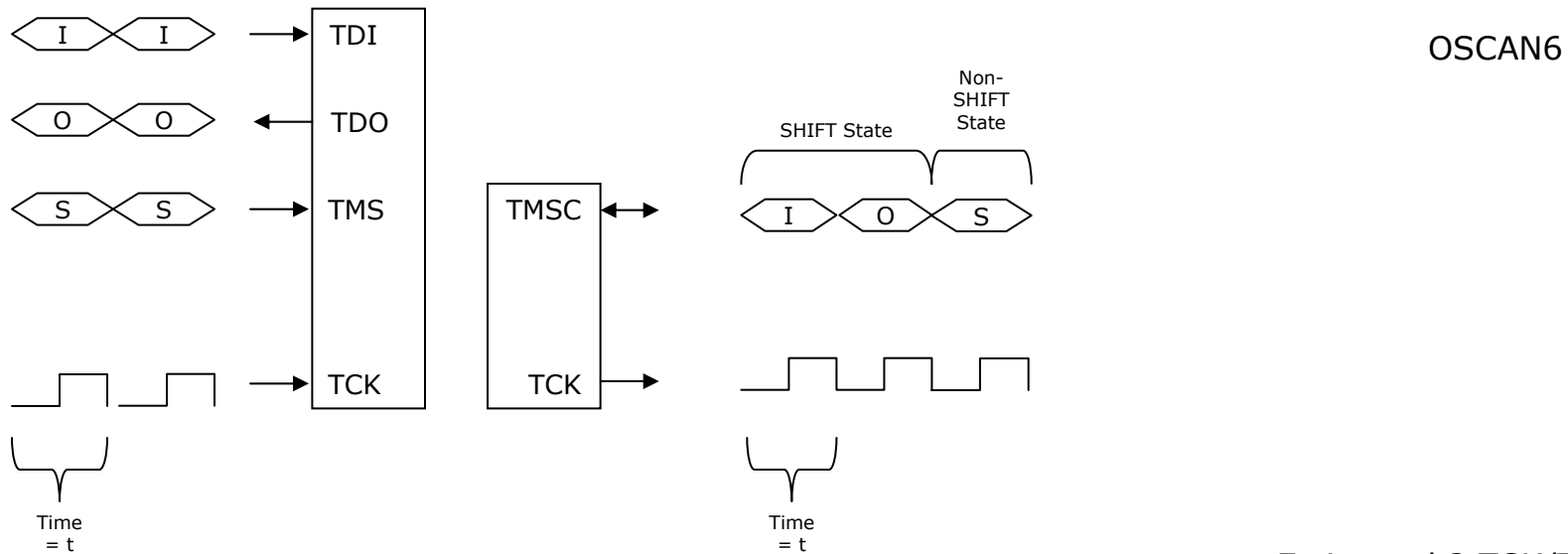
Estimated 4 TCK/TAP state

Scan Format	Shift TAP states				Non-Shift TAP States			
	TDO	LRDY	TMS	nTDI	TDO	LRDY	TMS	nTDI
OScan0	X	X	X	X	X	X	X	X

- OSCAN0 provides no optimization, but provides maximum compatibility

Note: DTS Supplied TCK

Optimization: IEEE1149.1 Compliant TAP



Estimated 2 TCK/TAP state

Scan Format	Shift TAP states				Non-Shift TAP States			
	TDO	LRDY	TMS	nTDI	TDO	LRDY	TMS	nTDI
OScan6	X	--		X	--	--	X	--

- If a IEEE1149.1 TAP is used, then Link Ready is not needed
- In the SHIFT state, TMS is not needed, so it can be optimized out
- In the non-SHIFT states, TMS is needed to move through the state machine. But neither TDO or TDI is needed

Note: DTS Supplied TCK

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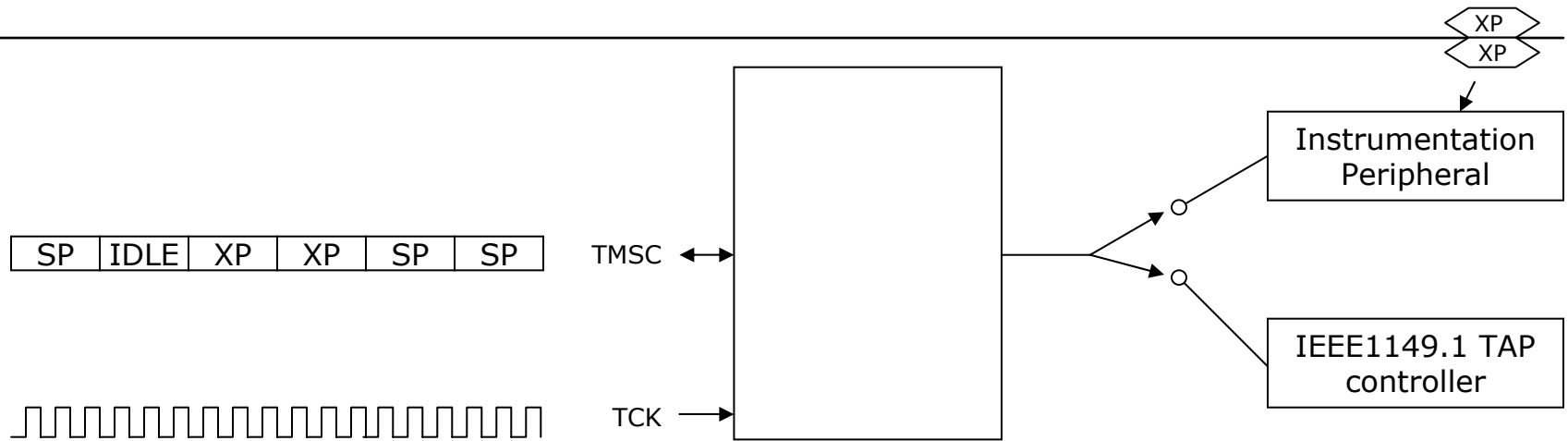
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Gateway for advanced technology and instrumentation

- ◆ Transport packet type is added to support:
 - Background Data Transfers (BDX)
 - Custom Data Transfers (CDX)
- ◆ When BDX is enabled:
 - During link IDLE time, instrumentation data is transmitted
 - Transport packets are attached to the IDLE, PAUSE, or UPDATE states
 - DTC to target, target to DTC , Bi-Directional or custom transfers
 - Non-scan data is transferred (ex: instrumentation data)
 - TAP.7 controller manages the TMSC pin, and input/output bandwidth is fixed and the transfer is limited to a single client.
- ◆ When CDX is enabled:
 - Input/output bandwidth allocation is variable and the transfer may be single client, multi-client, or client to client.
 - Client manages the TMSC pin

BDX in Operation



- BDX utilizes the pins in a manner similar to a Time Division Multiplex switch:
 - Following the IDLE, PAUSE, or UPDATE states, it transmits BDX information
 - Then the BDX burst will be followed by scan packets or another BDX burst if no scan activity is required

1149.7 Summary

- ◆ Do More with fewer pins
- ◆ New Connection topologies
- ◆ Backwards compatible with Si and Tools
- ◆ Gateway for advanced technology and instrumentation
- ◆ Preserve performance and capability
- ◆ Implement only what you need

Thank You!



About the Author

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