

# **X-Canceling MISR - New Approach for X-Tolerant Output Compaction**

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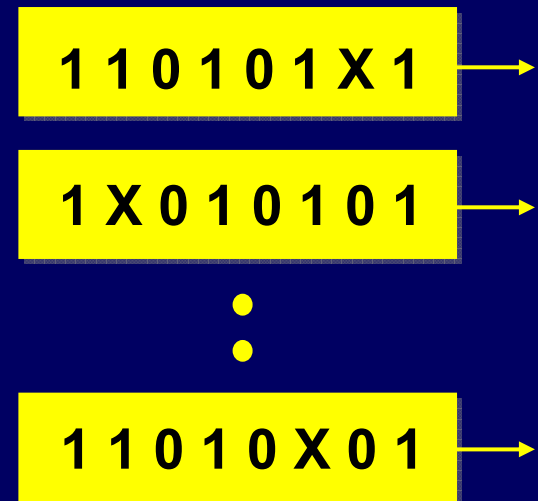


# INTRODUCTION

## Many Sources of Unknown X's in Output Response

- Uninitialized Memory Elements
- Bus Contention
- Floating Tri-States
- Multi-cycle Paths
- Etc.

### Scan Chains



## Conventional Scan Testing

- Easy to Handle by Masking on Tester

## Major Issue for Test Compression and Logic BIST

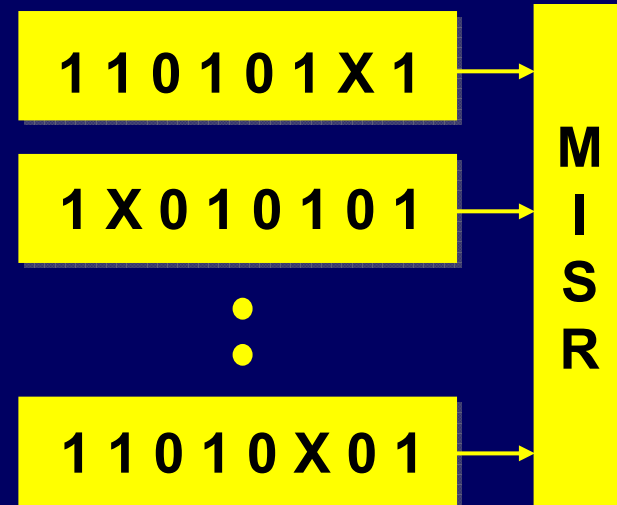
- X's Corrupt Final Signature
- Prevents Observation of Other Scan Cells

# INTRODUCTION

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- Bus Contention
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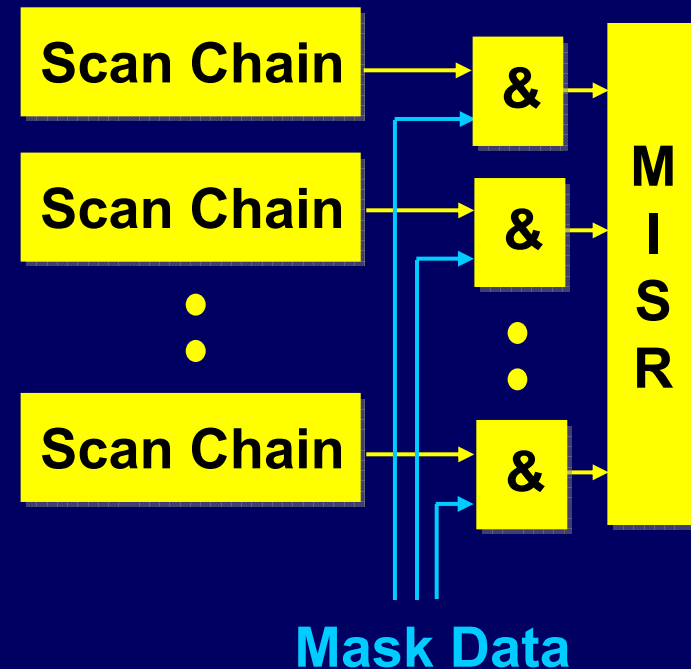
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- X's Corrupt Final Signature
- Prevents Observation of Other Scan Cells

# HANDLING X's

## Schemes for Handling X's

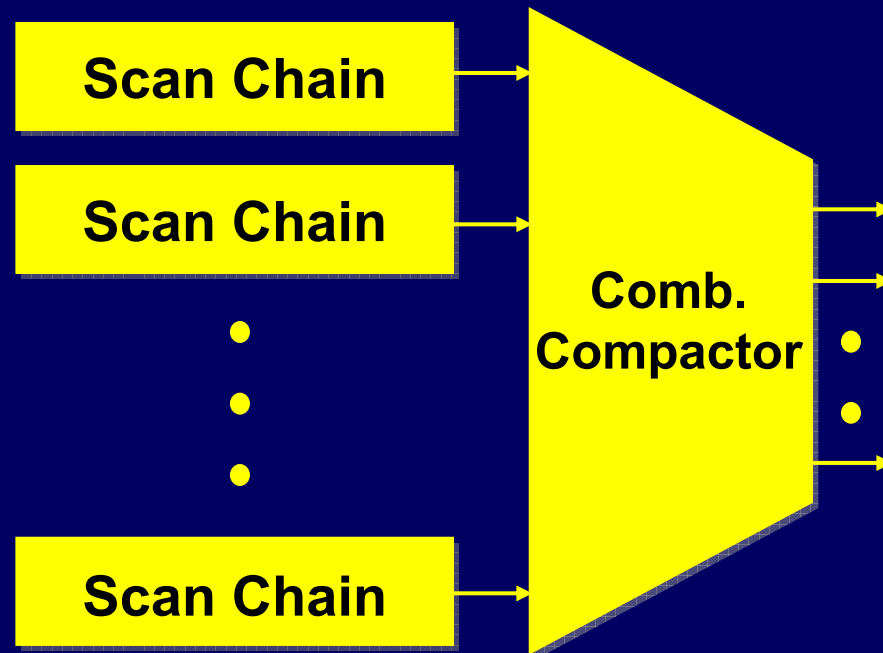
- X-Bounding
  - Insert DFT to Prevent X's from Propagating to Output
- X-Masking
  - Mask X's at Input to Compactor
  - Mask Data Required
- X-Tolerant Compactor



# X-COMPACT

## Combinational Compactor [Mitra & Kim, TCAD 04]

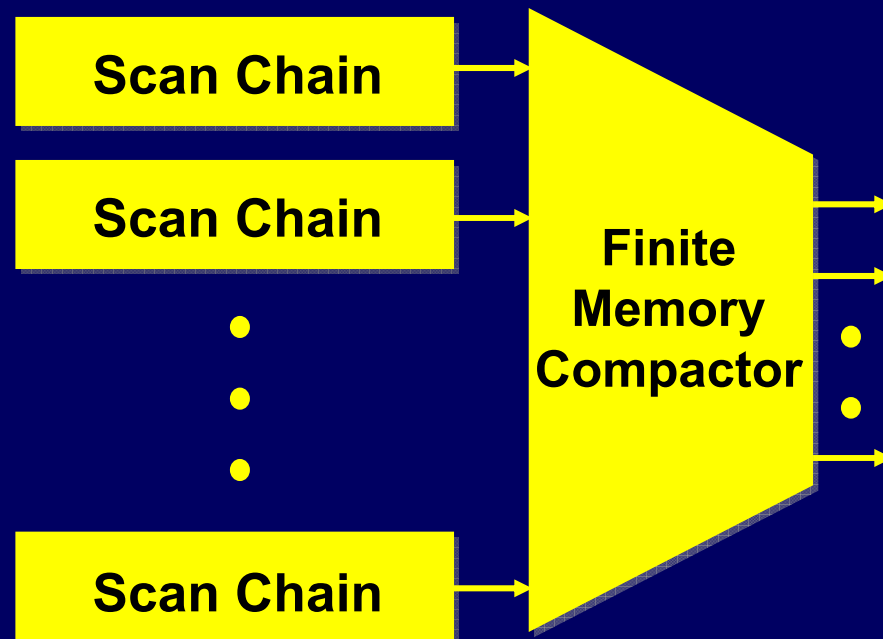
- Tolerates One X per Scan Slice
- Detects 1, 2, or Any Odd Errors
- Corrupted Outputs Masked on Tester



# CONVOLUTIONAL COMPACTOR

Convolutional Compactor [Rajski, *et al.*, TCAD 05]

- **Combinational Compactors Feeding Multiple Shift Registers**
- **Tradeoff Compaction Ratio with Number of X's Tolerated in Window of Scan Slices**



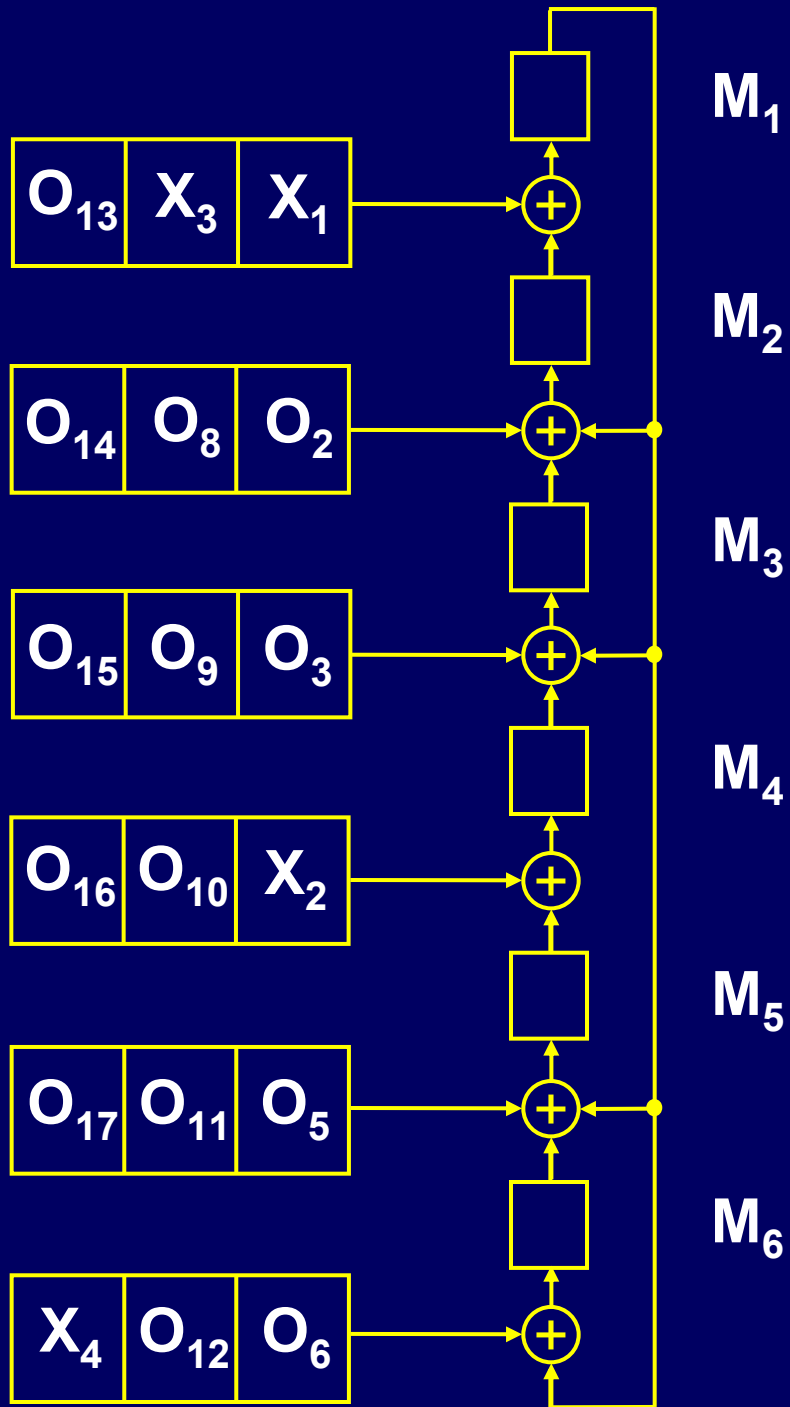
# X-CANCELING MISR

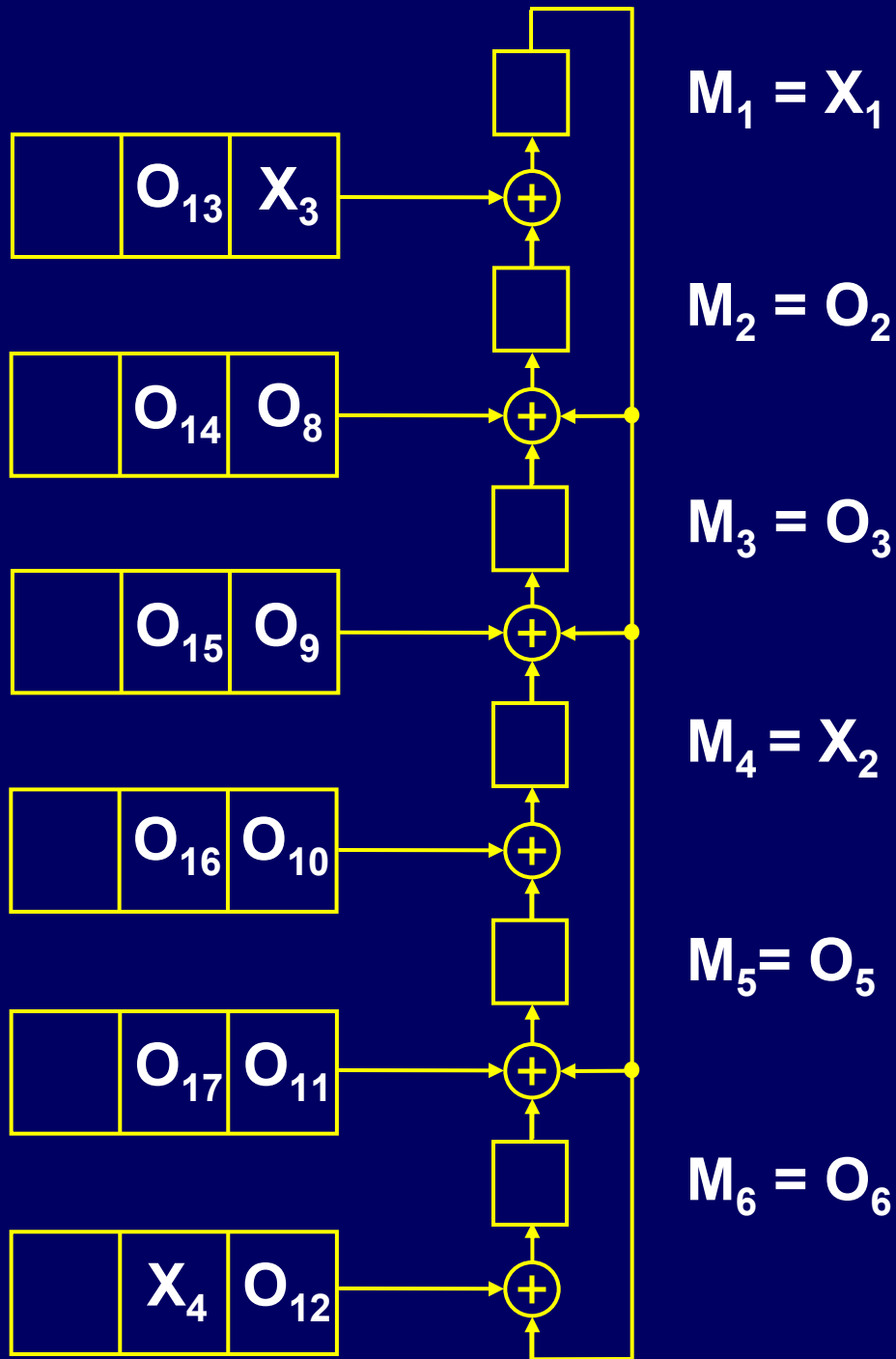
## X-Tolerant MISR

- Based on Canceling Out X's in Signature
  - Using Information from Symbolic Simulation
- For  $m$ -bit MISR
  - Each Signature Can Compact Up to  $k$  X's with Error Coverage Equivalent to  $m-k$  Bit MISR without X's

## Example

- 256-Bit MISR Can Tolerate up to 240 X's
  - Error Coverage Equivalent to 16 Bit MISR without X's





$$M_1 = X_1$$

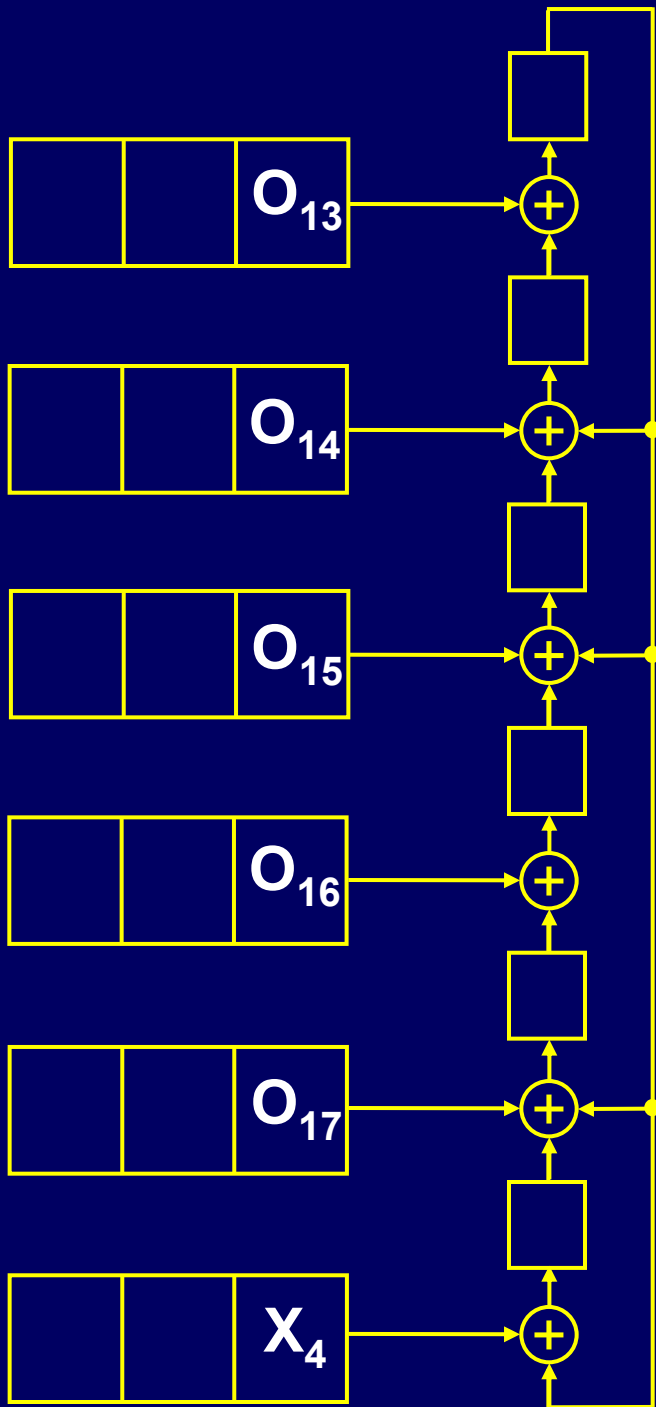
$$M_2 = O_2$$

$$M_3 = O_3$$

$$M_4 = X_2$$

$$M_5 = O_5$$

$$M_6 = O_6$$



$$M_1 = O_2 \oplus X_3$$

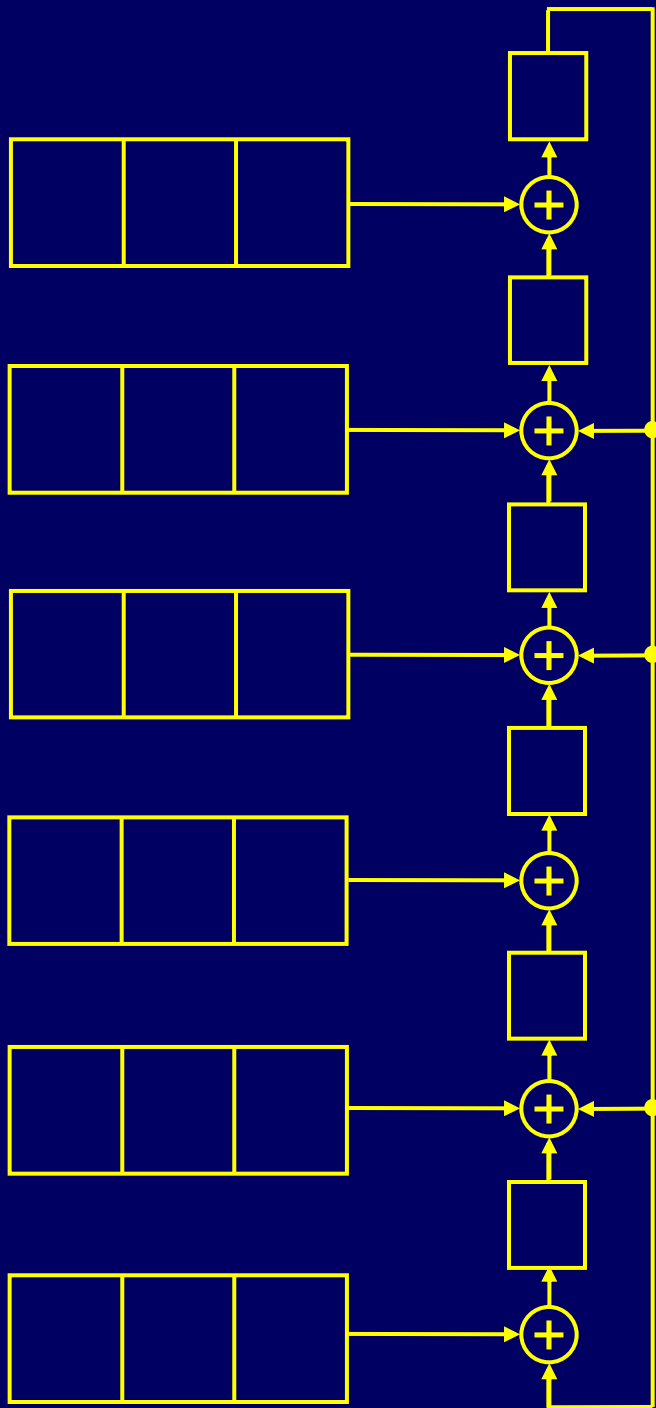
$$M_2 = O_3 \oplus X_1 \oplus O_8$$

$$M_3 = X_1 \oplus X_2 \oplus O_9$$

$$M_4 = O_5 \oplus O_{10}$$

$$M_5 = O_6 \oplus X_1 \oplus O_{11}$$

$$M_6 = X_1 \oplus O_{12}$$



$$M_1 = X_1 \oplus O_3 \oplus O_8 \oplus O_{13}$$

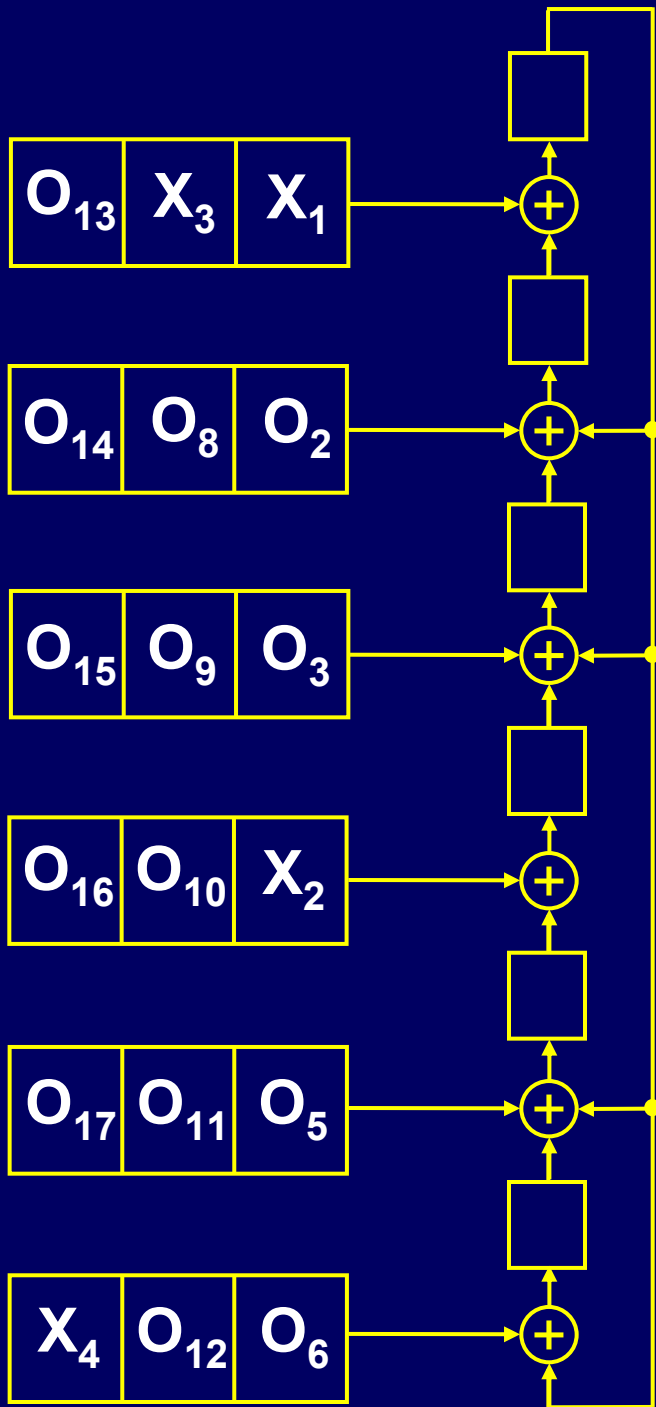
$$M_2 = X_1 \oplus O_2 \oplus X_2 \oplus X_3 \oplus O_9 \oplus O_{14}$$

$$M_3 = O_2 \oplus O_5 \oplus X_3 \oplus O_{10} \oplus O_{15}$$

$$M_4 = X_1 \oplus O_6 \oplus O_{11} \oplus O_{16}$$

$$M_5 = X_1 \oplus O_2 \oplus X_3 \oplus O_{12} \oplus O_{17}$$

$$M_6 = O_2 \oplus X_3 \oplus X_4$$



$$M_1 = X_1 \oplus O_3 \oplus O_8 \oplus O_{13}$$

$$M_2 = X_1 \oplus O_2 \oplus X_2 \oplus X_3 \oplus O_9 \oplus O_{14}$$

$$M_3 = O_2 \oplus O_5 \oplus X_3 \oplus O_{10} \oplus O_{15}$$

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$$M_5 = X_1 \oplus O_2 \oplus X_3 \oplus O_{12} \oplus O_{17}$$

$$M_6 = O_2 \oplus X_3 \oplus X_4$$



# ALIASING WHEN COMPACTING X's

Probability Error Results in Valid Fault-Free Signature

$$\frac{\text{Valid Fault-Free Signatures}}{\text{Total Possible Signatures}} = \frac{2^{(\text{Number X's})}}{2^{(\text{MISR Bits})}}$$

Example

- 256 Bit MISR Compacting 236 X's

$$\text{Probability of Aliasing} = \frac{2^{236}}{2^{256}} = \frac{1}{2^{20}}$$

- Equivalent to Using a 20-Bit MISR without X's

# LINEARLY DEPENDENT COMBINATIONS

## Linearly Dependent Combinations of MISR Bits

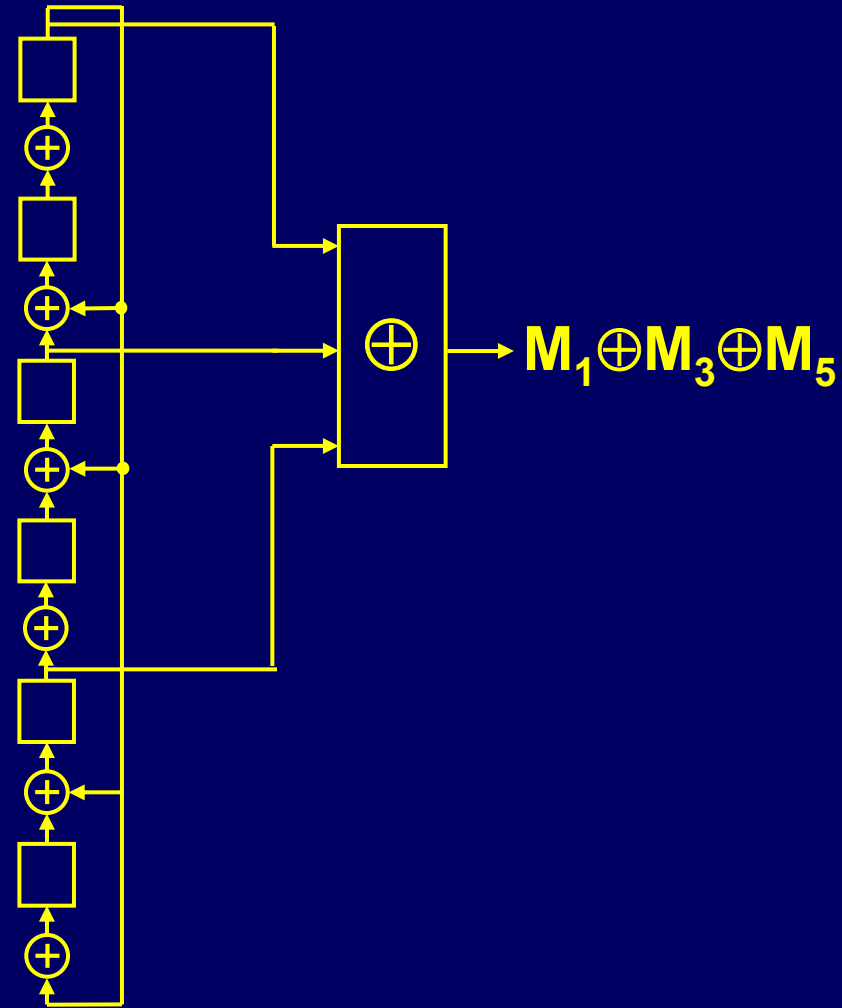
- No Dependence on  $X$ 's
- Guaranteed to Exist When More MISR Bits Than  $X$ 's

$$\begin{array}{l} M_1 = X_1 \\ M_2 = X_1 \oplus X_2 \oplus X_3 \\ M_3 = X_3 \\ M_4 = X_1 \\ M_5 = X_1 \oplus X_3 \\ M_6 = X_3 \oplus X_4 \end{array} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \xrightarrow{\text{Gaussian Elimination}} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{array}{l} M_1 \\ M_1 \oplus M_2 \oplus M_3 \\ M_3 \\ M_3 \oplus M_6 \\ M_1 \oplus M_3 \oplus M_5 \\ M_1 \oplus M_4 \end{array}$$

$$M_1 = X_1 \oplus O_3 \oplus O_8 \oplus O_{13}$$

$$M_3 = O_2 \oplus O_5 \oplus X_3 \oplus O_{10} \oplus O_{15}$$

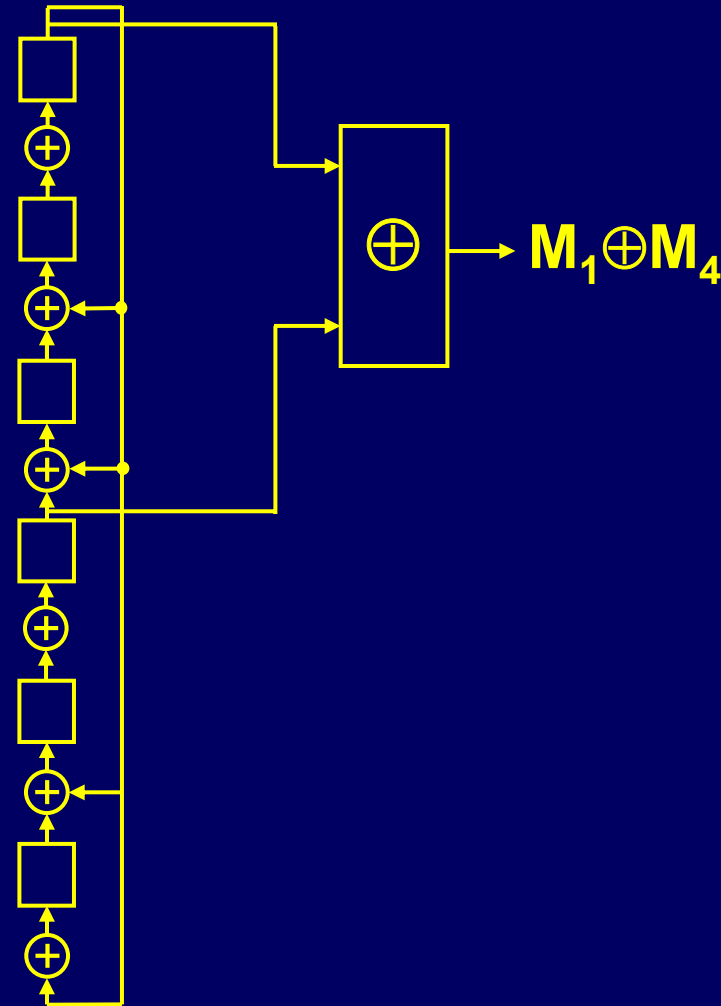
$$M_5 = X_1 \oplus O_2 \oplus X_3 \oplus O_{12} \oplus O_{17}$$



1	0	0	0	$M_1$
0	1	0	0	$M_1 \oplus M_2 \oplus M_3$
0	0	1	0	$M_3$
0	0	0	1	$M_3 \oplus M_6$
0	0	0	0	$M_1 \oplus M_3 \oplus M_5 = O_3 \oplus O_5 \oplus O_8 \oplus O_{10} \oplus O_{12} \oplus O_{13} \oplus O_{15} \oplus O_{17}$
0	0	0	0	$M_1 \oplus M_4$

$$M_1 = X_1 \oplus O_3 \oplus O_8 \oplus O_{13}$$

$$M_4 = X_1 \oplus O_6 \oplus O_{11} \oplus O_{16}$$



1	0	0	0	$M_1$
0	1	0	0	$M_1 \oplus M_2 \oplus M_3$
0	0	1	0	$M_3$
0	0	0	1	$M_3 \oplus M_6$
0	0	0	0	$M_1 \oplus M_3 \oplus M_5$
0	0	0	0	$M_1 \oplus M_4 = O_3 \oplus O_6 \oplus O_8 \oplus O_{11} \oplus O_{13} \oplus O_{16}$

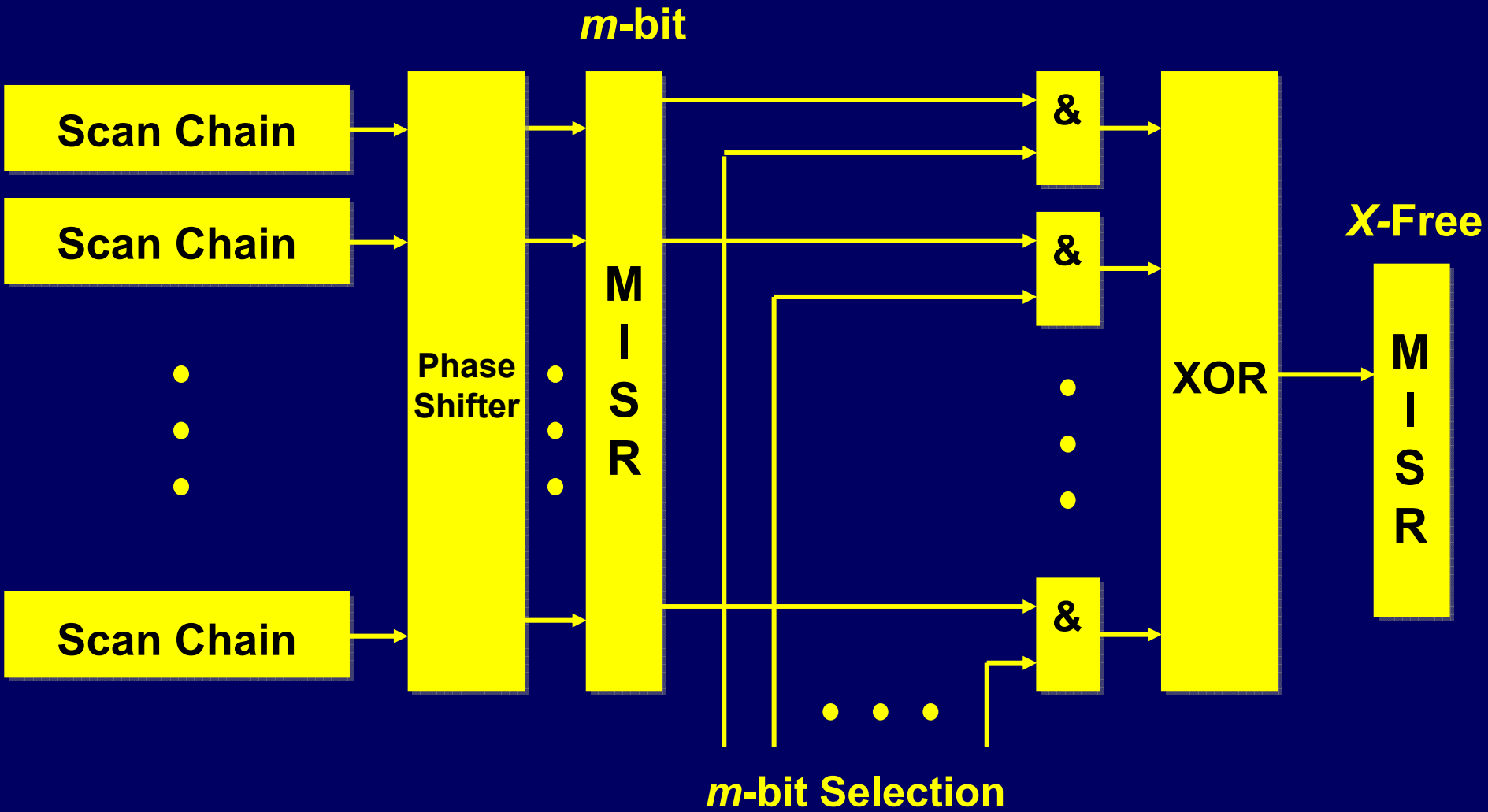
# ERROR COVERAGE

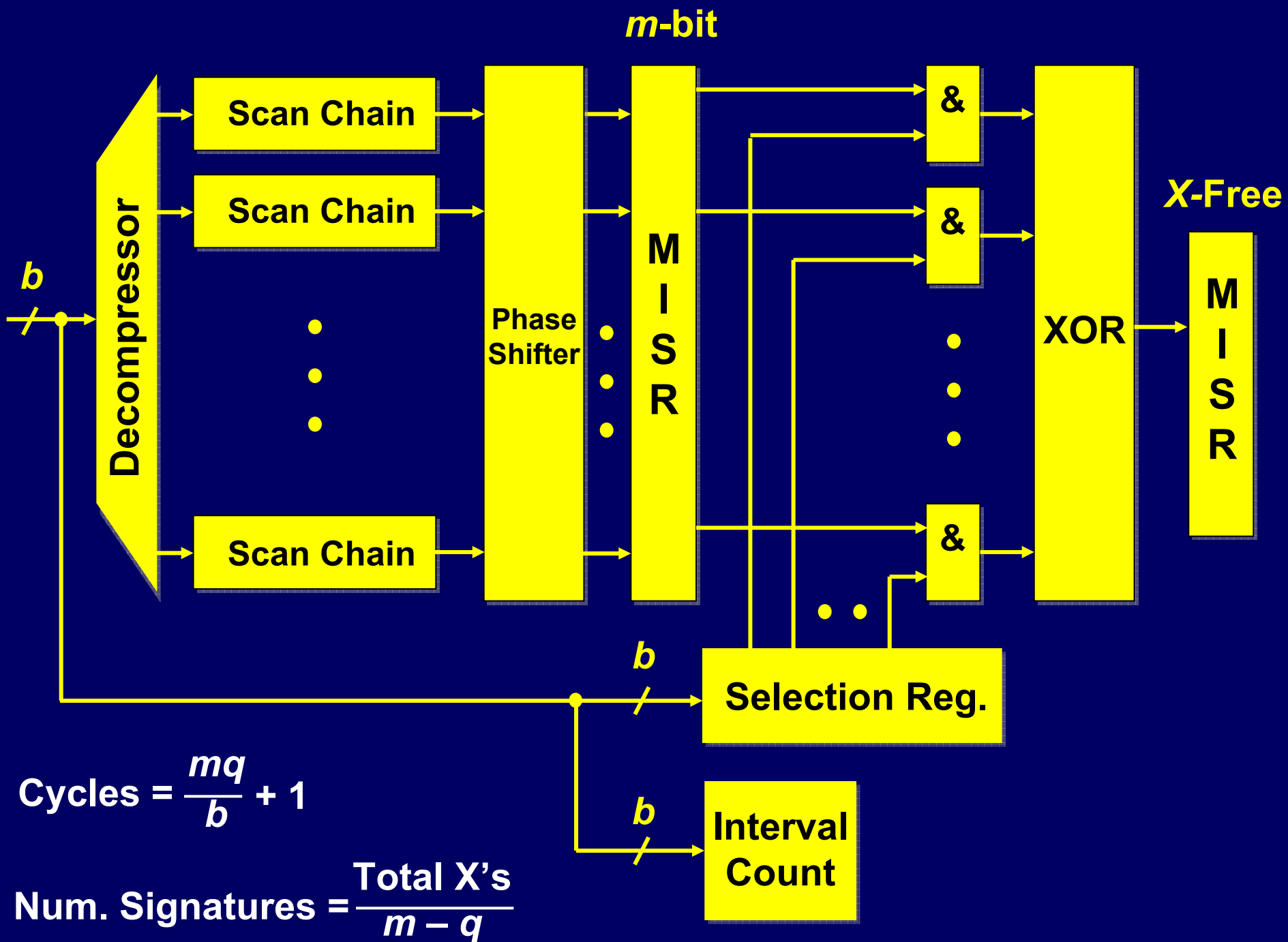
$$\text{Error Coverage} = 1 - 2^{-(\text{Checked Combs})}$$

$$\text{X's Tolerated Per Signature} = \text{MISR Bits} - \text{Checked Combs}$$

1	50%
2	75%
3	87.5%
4	93.75%
5	96.88%
6	98.44%
7	99.2%
8	99.6%
9	99.8%
10	99.9%
11	99.95%
12	99.97%
13	99.99%
14	99.994%
15	99.997%
16	99.998%

# ARCHITECTURE





# ANALYSIS

$$\text{Num. Signatures} = \frac{\text{Total X's}}{m - q}$$

$$\text{Total Data} = (mq)(\text{Num. Signatures}) = \frac{(mq)(\text{Total X's})}{m - q}$$

If  $q \ll m$

- Total Data  $\approx (q)(\text{Total X's})$

$q$	Coverage
1	50%
2	75%
3	87.5%
4	93.75%
5	96.88%
6	98.44%
7	99.2%
8	99.6%
9	99.8%
10	99.9%
11	99.95%
12	99.97%
13	99.99%
14	99.994%
15	99.997%
16	99.998%

# ANALYSIS

Total Data  $\approx (q)(\text{Total X's})$

Tester Storage Independent of

- Design Size
- Scan Architecture
  - Number Scan Chains
  - Scan Length
  - Scan Cells
- Number Test Vectors

Error Coverage Independent of

- Distribution of X's

$q$	Coverage
1	50%
2	75%
3	87.5%
4	93.75%
5	96.88%
6	98.44%
7	99.2%
8	99.6%
9	99.8%
10	99.9%
11	99.95%
12	99.97%
13	99.99%
14	99.994%
15	99.997%
16	99.998%

# COMPARISON

## X-Compact [Mitra & Kim, TCAD 04]

- **Combinational Compactor**
- **Tester Channels  $\approx \log_2(\text{Scan Chains})$**

## Tester Storage

$$= 2 (\text{Num. Slices}) \log_2(\text{Scan Chains})$$

$$= 2 (\text{Num. Vectors}) (\text{Scan Length}) \log_2(\text{Scan Chains})$$

## Error Coverage

- **Tolerates One X per Scan Slice**
- **Detects 1, 2, and Odd Errors per Scan Slice**

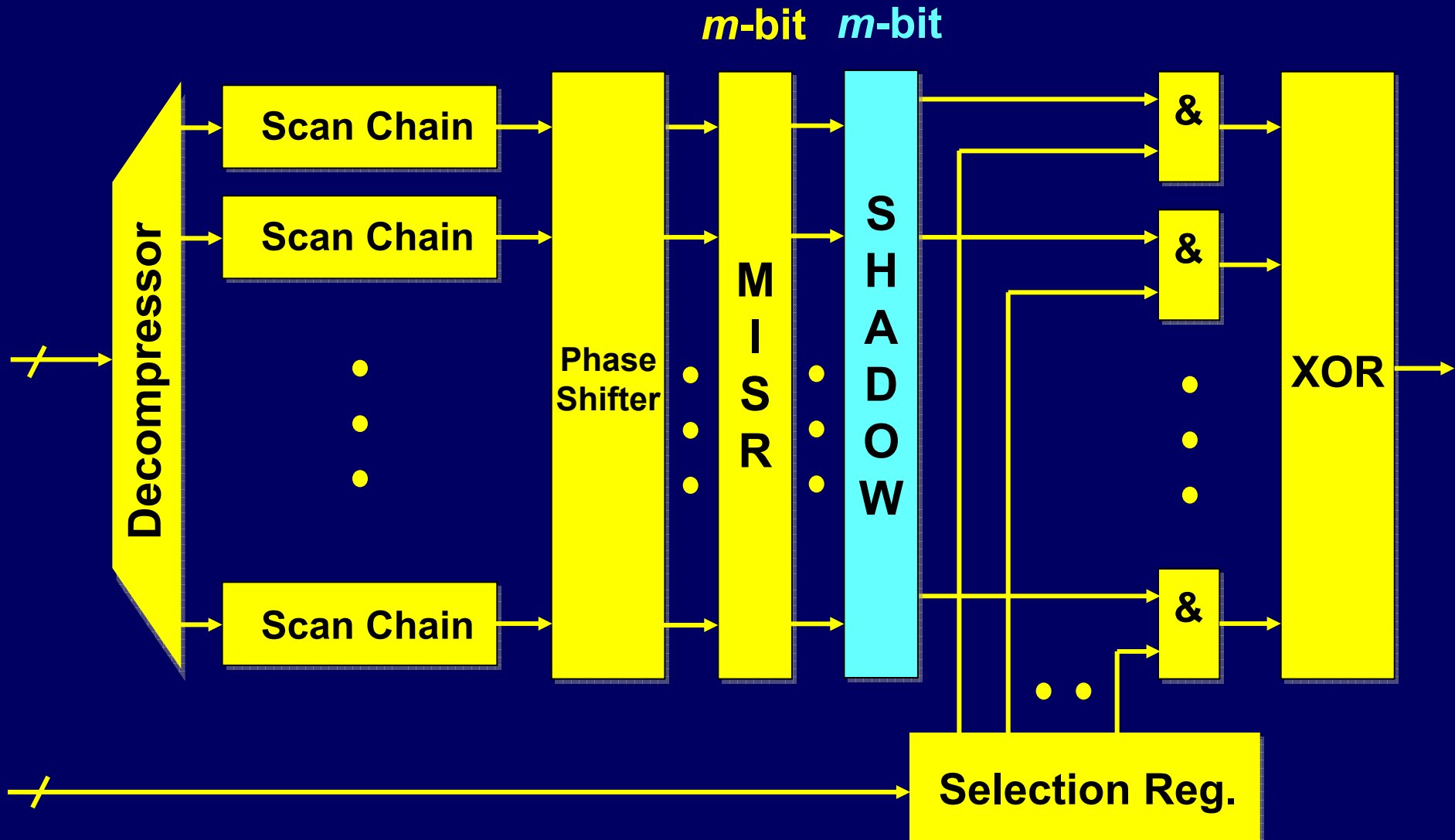
# COMPARISON

% X's	Scan Chains	Slices w/more than One X	X-Compact		X-Canceling MISR	
			Outputs	Comp. Ratio	$q = 7$ 99.2% Cov.	$q = 12$ 99.97% Cov.
0.01%	1024	0.5%	13	79x	1390x	794x
	512	0.1%	12	43x	1390x	794x
0.05%	256	0.8%	11	23.3x	278x	159x
	128	0.2%	10	12.8x	278x	159x
0.1%	128	0.8%	10	12.8x	139x	79x
	64	0.2%	9	7.1x	139x	79x
0.5%	32	1.1%	7	4.6x	27.8x	15.9x
	16	0.3%	6	2.7x	27.8x	15.9x
1%	16	1.1%	6	2.7x	13.9x	7.9x
	8	0.3%	5	1.6x	13.9x	7.9x

# FAULT COVERAGE

Circuit	X-Canceled Combinations ( $q$ )	Error Coverage	Fault Coverage
s13207	7	99.2%	99.2%
	9	99.8%	99.8%
	11	99.95%	100%
s15850	7	99.2%	99.2%
	9	99.8%	99.9%
	11	99.95%	100%
s38417	7	99.2%	99.4%
	9	99.8%	99.9%
	12	99.97%	100%
s38584	7	99.2%	99.4%
	9	99.8%	99.95%
	12	99.97%	100%

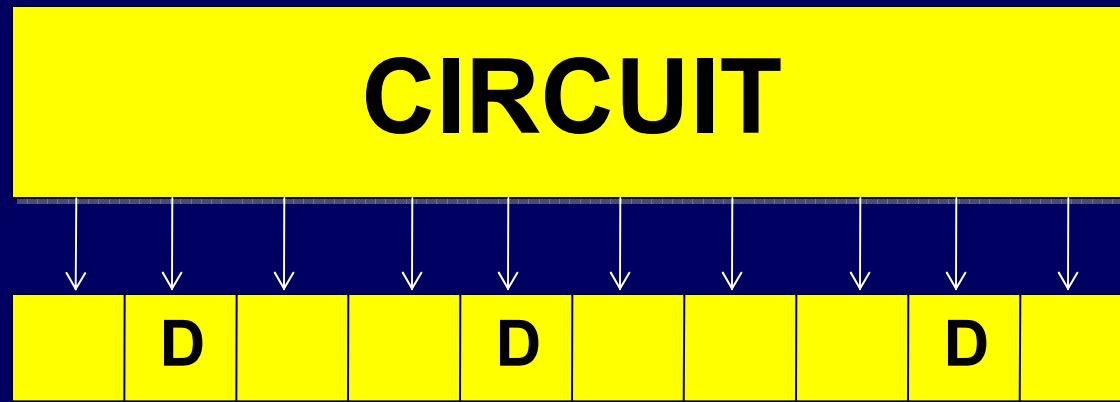
# CONTINUOUS SCAN SHIFTING



# COMPARISON

% X's	Scan Chains	Slices w/more than One X	X-Compact		X-Canceling MISR	
			Outputs	Comp. Ratio	$q = 7$ 99.2% Cov.	$q = 12$ 99.97% Cov.
0.01%	1024	0.5%	13	79x	1390x	794x
	512	0.1%	12	43x	1390x	794x
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0.1%	128	0.8%	10	12.8x	139x	79x
	64	0.2%	9	7.1x	139x	79x
0.5%	32	1.1%	7	4.6x	27.8x	15.9x
	16	0.3%	6	2.7x	27.8x	15.9x
1%	16	1.1%	6	2.7x	13.9x	7.9x
	8	0.3%	5	1.6x	13.9x	7.9x

For a Particular Pattern  $i$



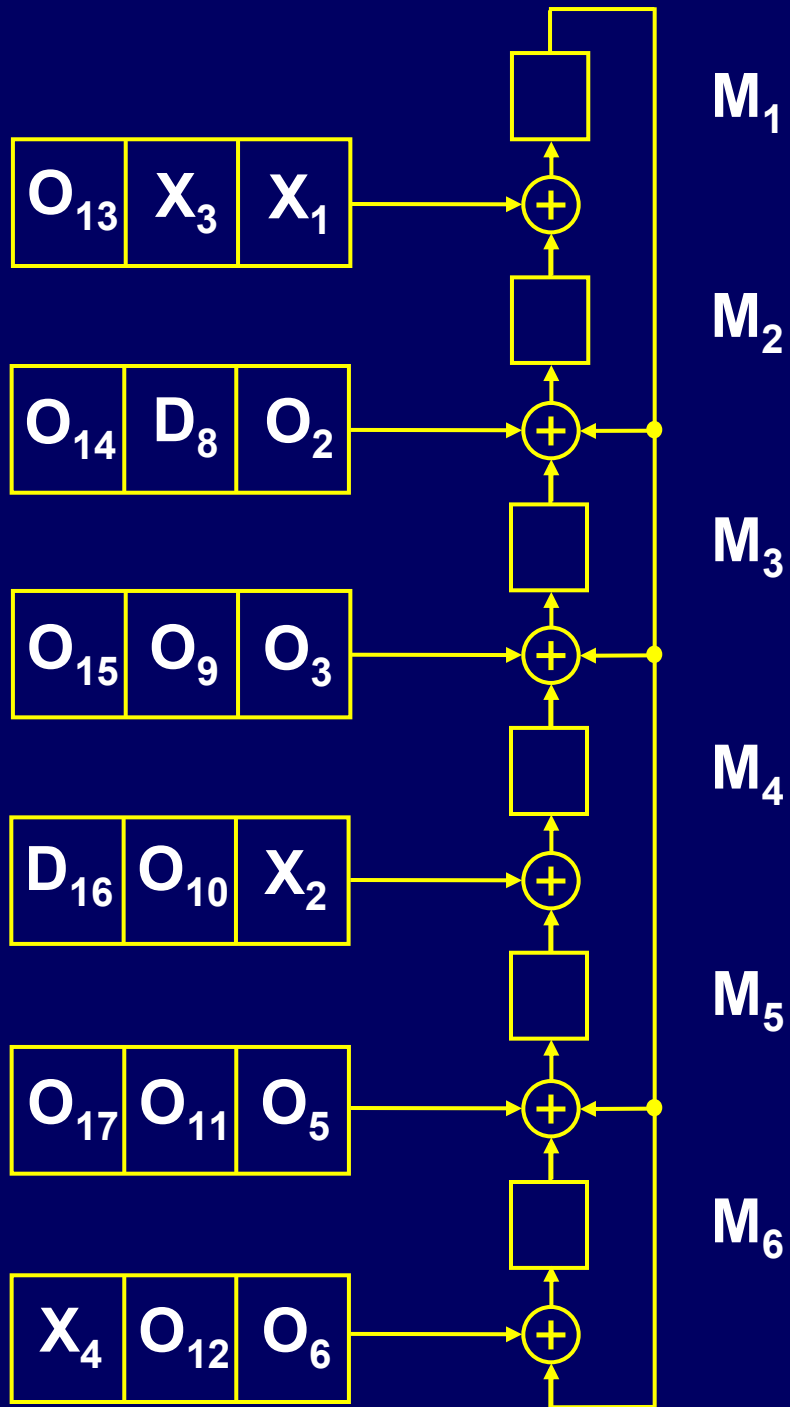
**D's** = Minimal Set of Scan Cells for which Observation Detects All Faults

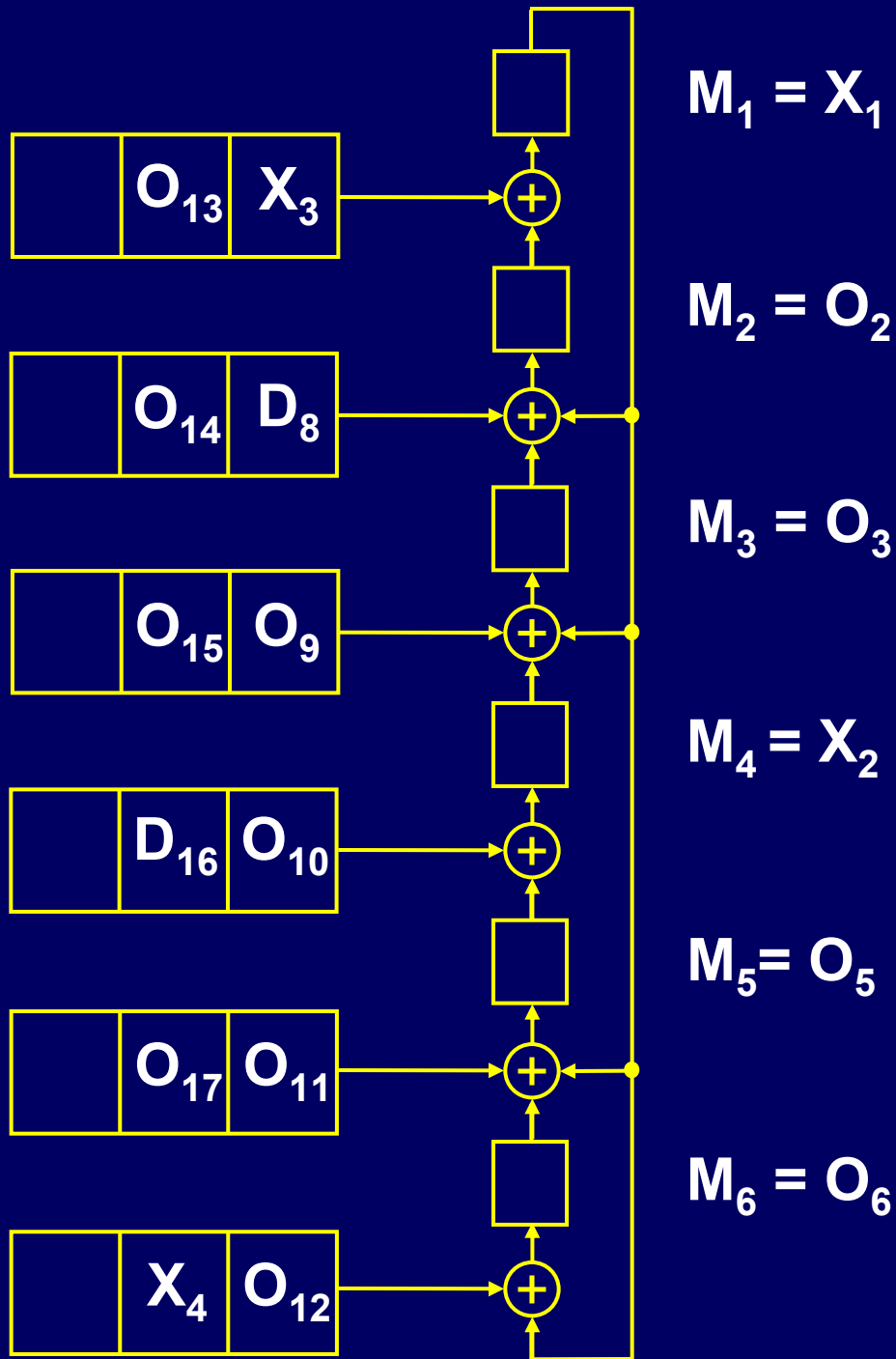
**Probabilistic Observation**

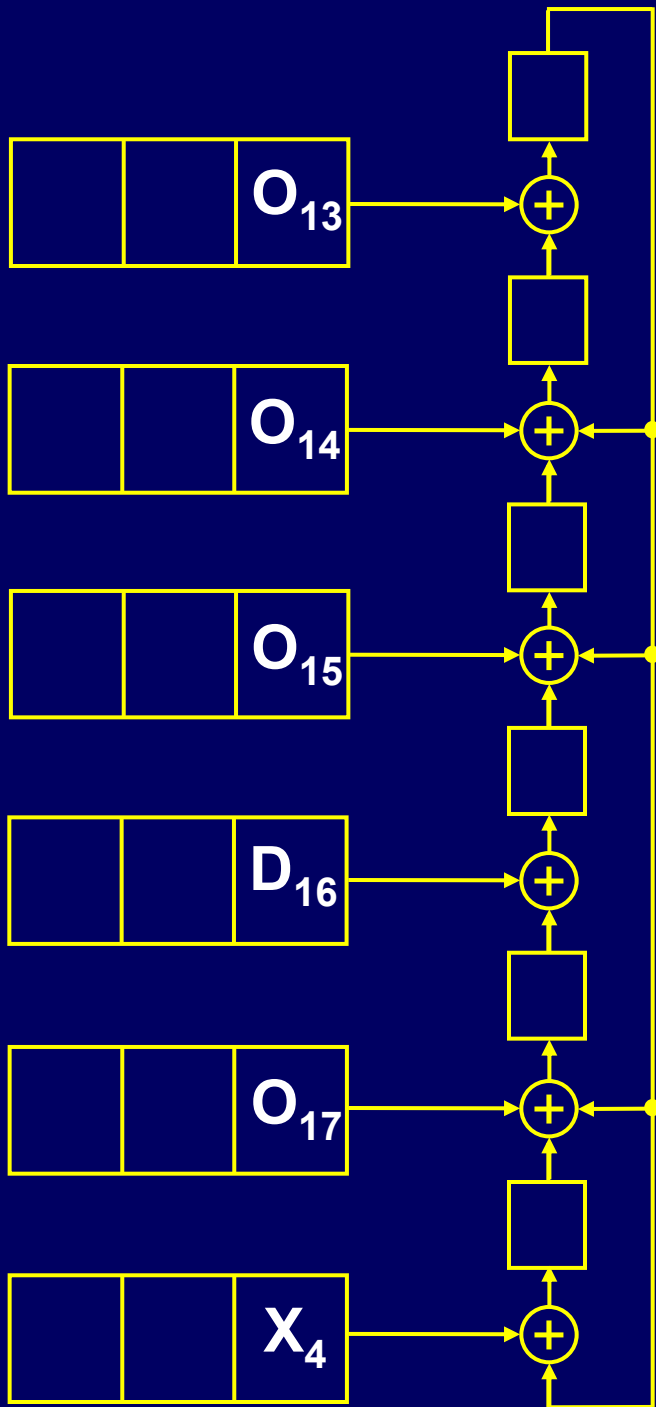
- High Coverage of All Scan Cells

**Deterministic Targeting of D's**

- Focus on Detecting D's







$$\mathbf{M}_1 = \mathbf{O}_2 \oplus \mathbf{X}_3$$

$$\mathbf{M}_2 = \mathbf{O}_3 \oplus \mathbf{X}_1 \oplus \mathbf{D}_8$$

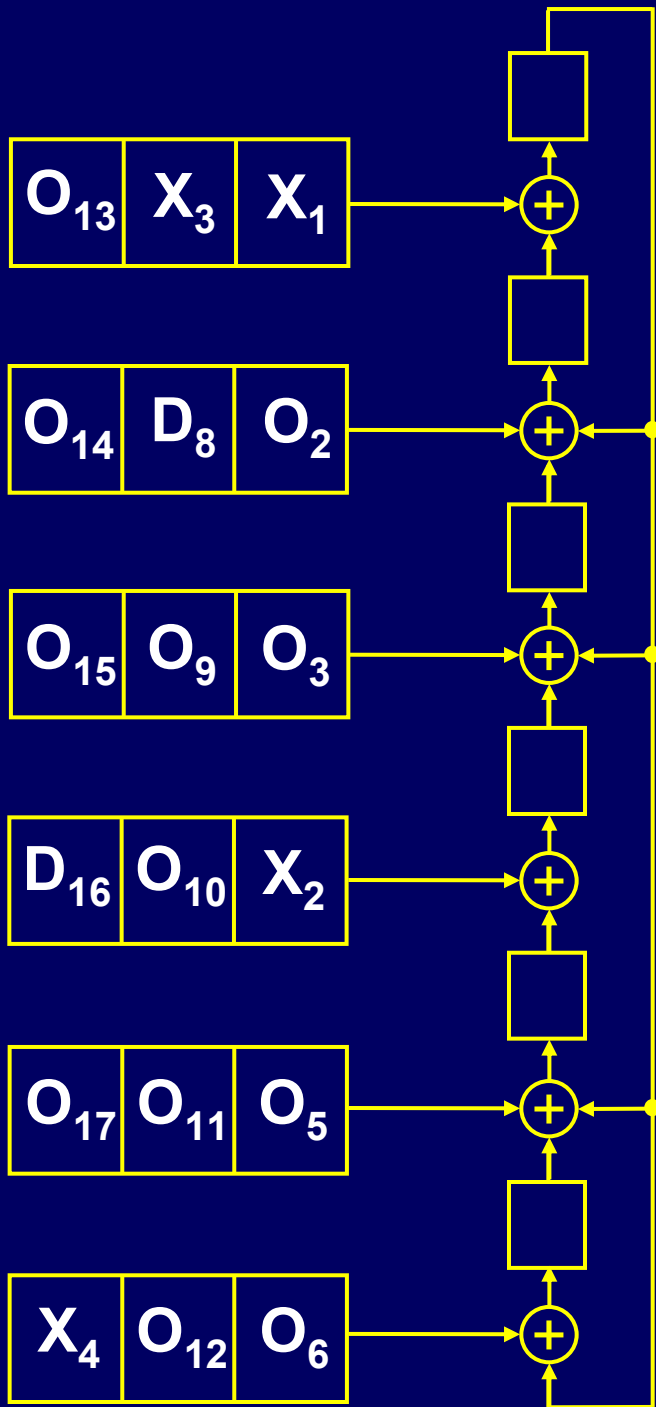
$$\mathbf{M}_3 = \mathbf{X}_1 \oplus \mathbf{X}_2 \oplus \mathbf{O}_9$$

$$\mathbf{M}_4 = \mathbf{O}_5 \oplus \mathbf{O}_{10}$$

$$\mathbf{M}_5 = \mathbf{O}_6 \oplus \mathbf{X}_1 \oplus \mathbf{O}_{11}$$

$$\mathbf{M}_6 = \mathbf{X}_1 \oplus \mathbf{O}_{12}$$





$$M_1 = X_1 \oplus O_3 \oplus D_8 \oplus O_{13}$$

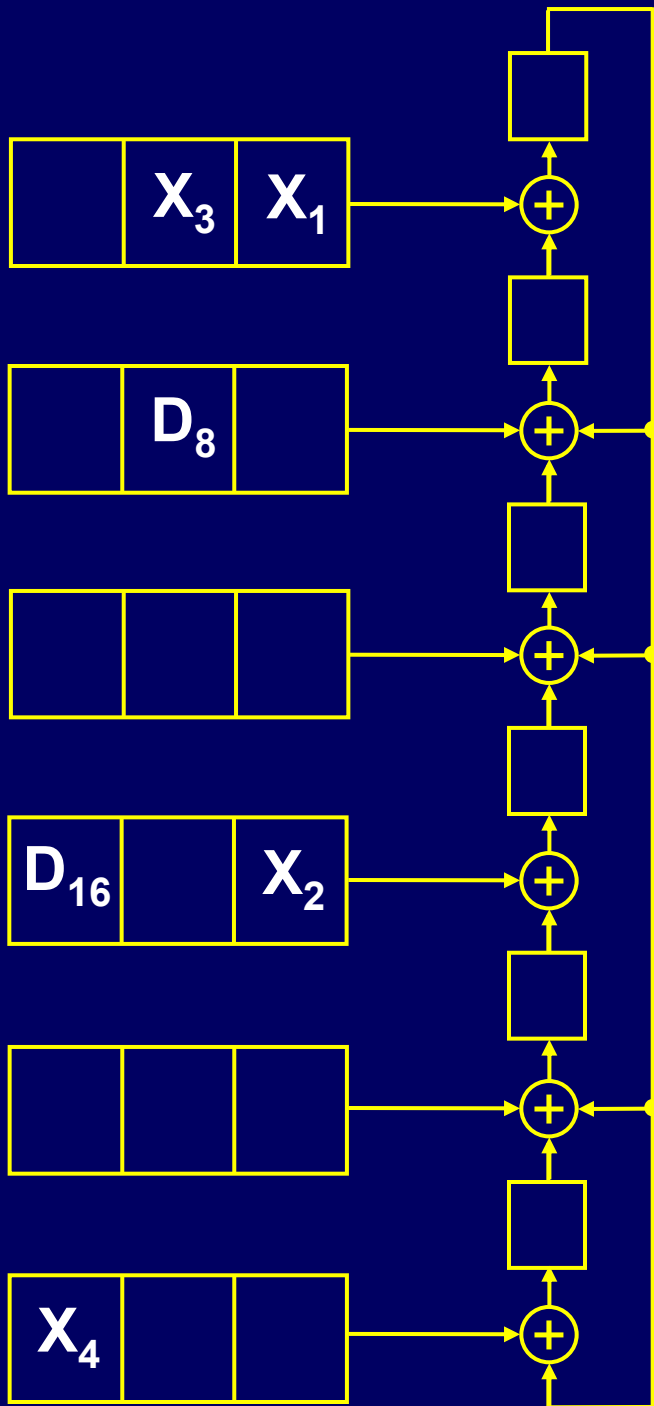
$$M_2 = X_1 \oplus O_2 \oplus X_2 \oplus X_3 \oplus O_9 \oplus O_{14}$$

$$M_3 = O_2 \oplus O_5 \oplus X_3 \oplus O_{10} \oplus O_{15}$$

$$M_4 = X_1 \oplus O_6 \oplus O_{11} \oplus D_{16}$$

$$M_5 = X_1 \oplus O_2 \oplus X_3 \oplus O_{12} \oplus O_{17}$$

$$M_6 = O_2 \oplus X_3 \oplus X_4$$



$$M_1 = X_1 \oplus D_8$$

$$M_2 = X_1 \oplus X_2 \oplus X_3$$

$$M_3 = X_3$$

$$M_4 = X_1 \oplus D_8$$

$$M_5 = X_1 \oplus X_3$$

$$M_6 = X_3 \oplus X_4$$





# ALIASING

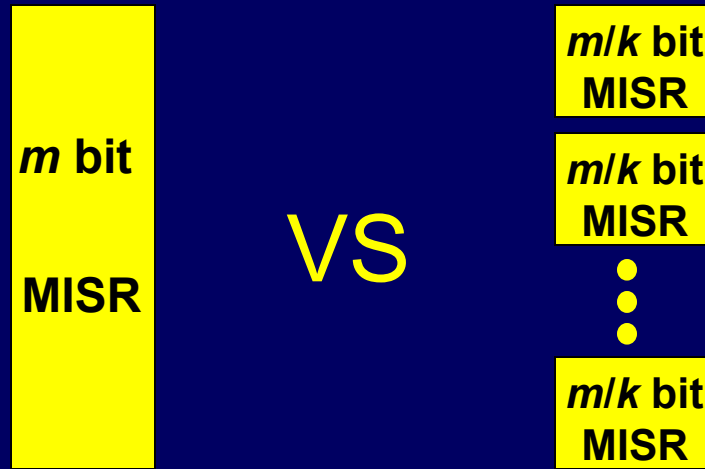
## Checking Only One Combination that Depends on All D's

- Odd Number of D's Have Errors
  - NO PROBLEM (Error Detected)
- Even Number of D's Have Errors
  - PROBLEM (All Errors Cancel Out)

## Solutions

- Check Multiple Combinations Rather than Just One
- Use Multiple MISR Design

# COMPARISON



Characteristics	Multiple Combinations	Multiple MISR
Number of MISR bit Combinations Checked	$k$ combinations from one $m$ bit MISR	1 combination each from $k$ $m/k$ bit MISRs
Storage Requirements	$k*m = km$ bits	$k*(m/k) = m$ bits
Error Coverage	$(1-2^{-k})$	$(1-2^{-k})^*$

\* If D's evenly distributed between MISRs

# MULTIPLE VS SINGLE MISR

Assuming All Error Combinations Equally Likely:

Combinations Checked ( $k$ )	Error Coverage	Bits on Tester for $m$ -bit MISR	Bits on Tester for $(m/k)$ -bit MISRs
1	50%	$m$	$m$
2	75%	$2m$	$m$
3	87.5%	$3m$	$m$
4	93.75%	$4m$	$m$

## Issues with Multiple MISRs

- X's and D's Not Evenly Distributed
  - One of  $(m/k)$  Bit MISR Gets Saturated Earlier
  - Multiple MISR Error Coverage Lower than Single MISR

# DESIGN EXAMPLE

m bits  
on  
tester

m

B  
I  
T

M  
I  
S  
R

Checking 1  
combination

Error Coverage

50%



# DESIGN EXAMPLE

m bits  
on  
tester

m  
B  
I  
T  
M  
I  
S  
R

Checking 1  
combination

Error Coverage  
50%



m bits  
on  
tester

m/2  
bit  
MISR

m/2  
bit  
MISR

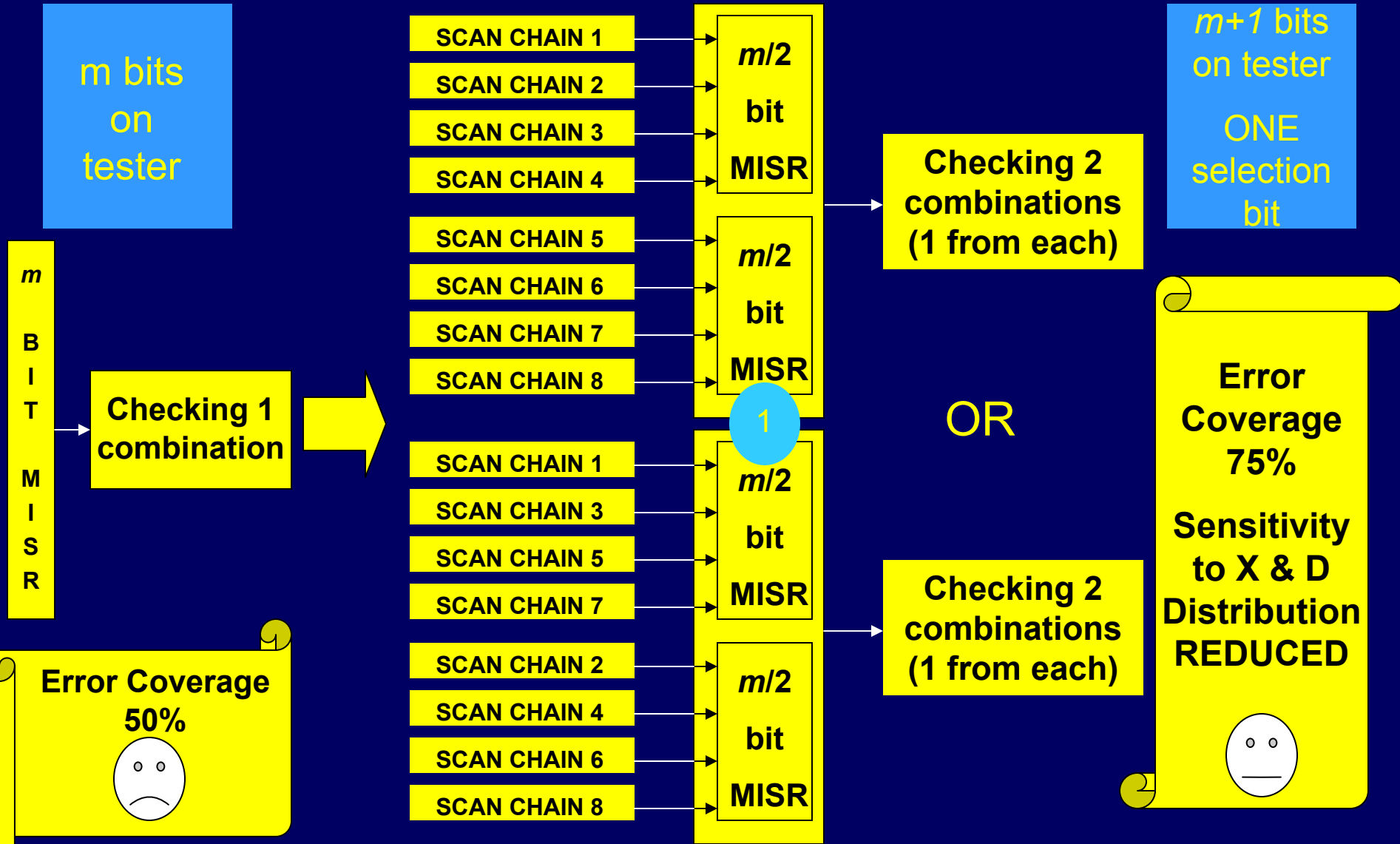
Checking 2  
combinations  
(1 from each)

Error  
Coverage  
75%

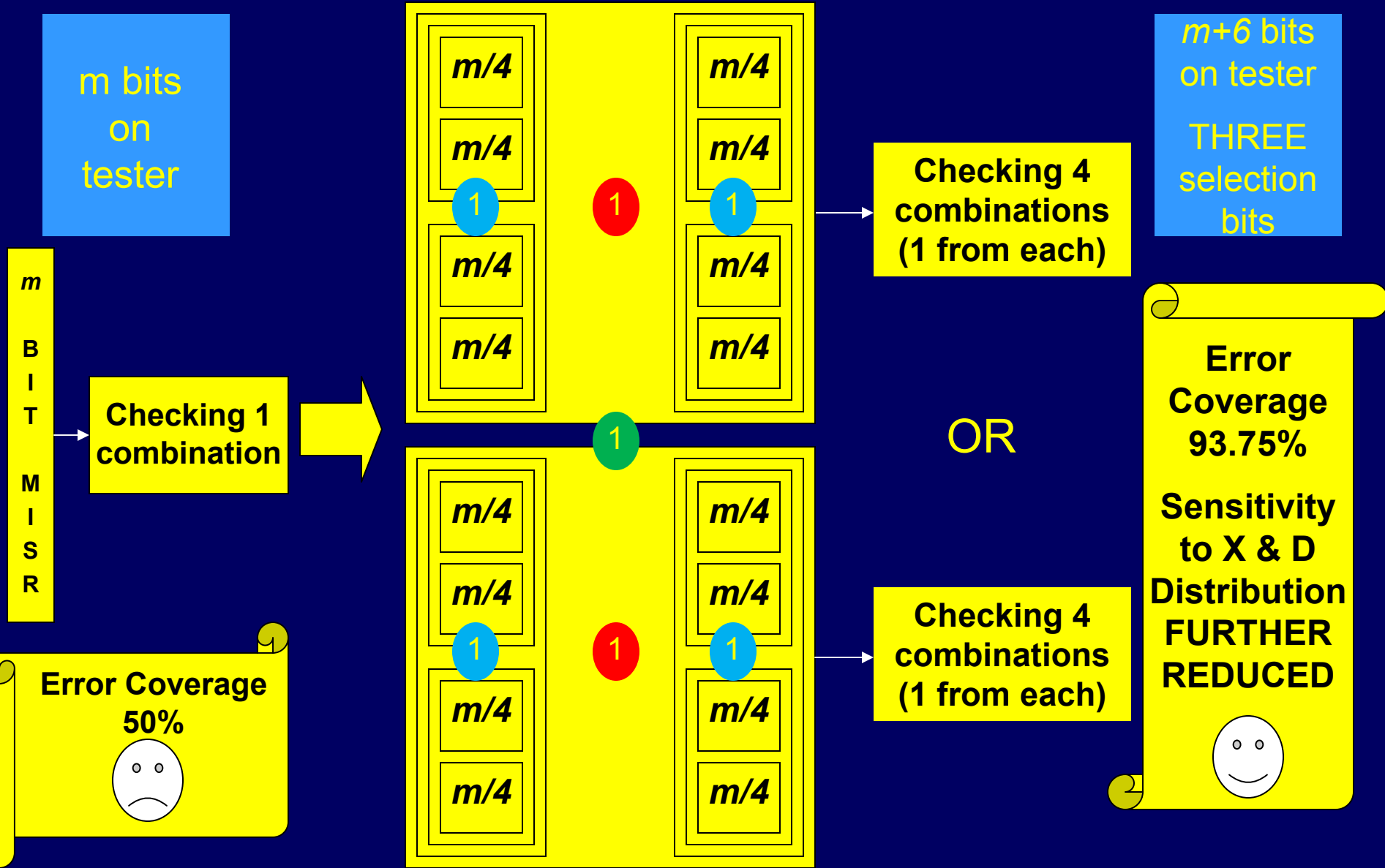
Sensitive to  
X & D  
Distribution



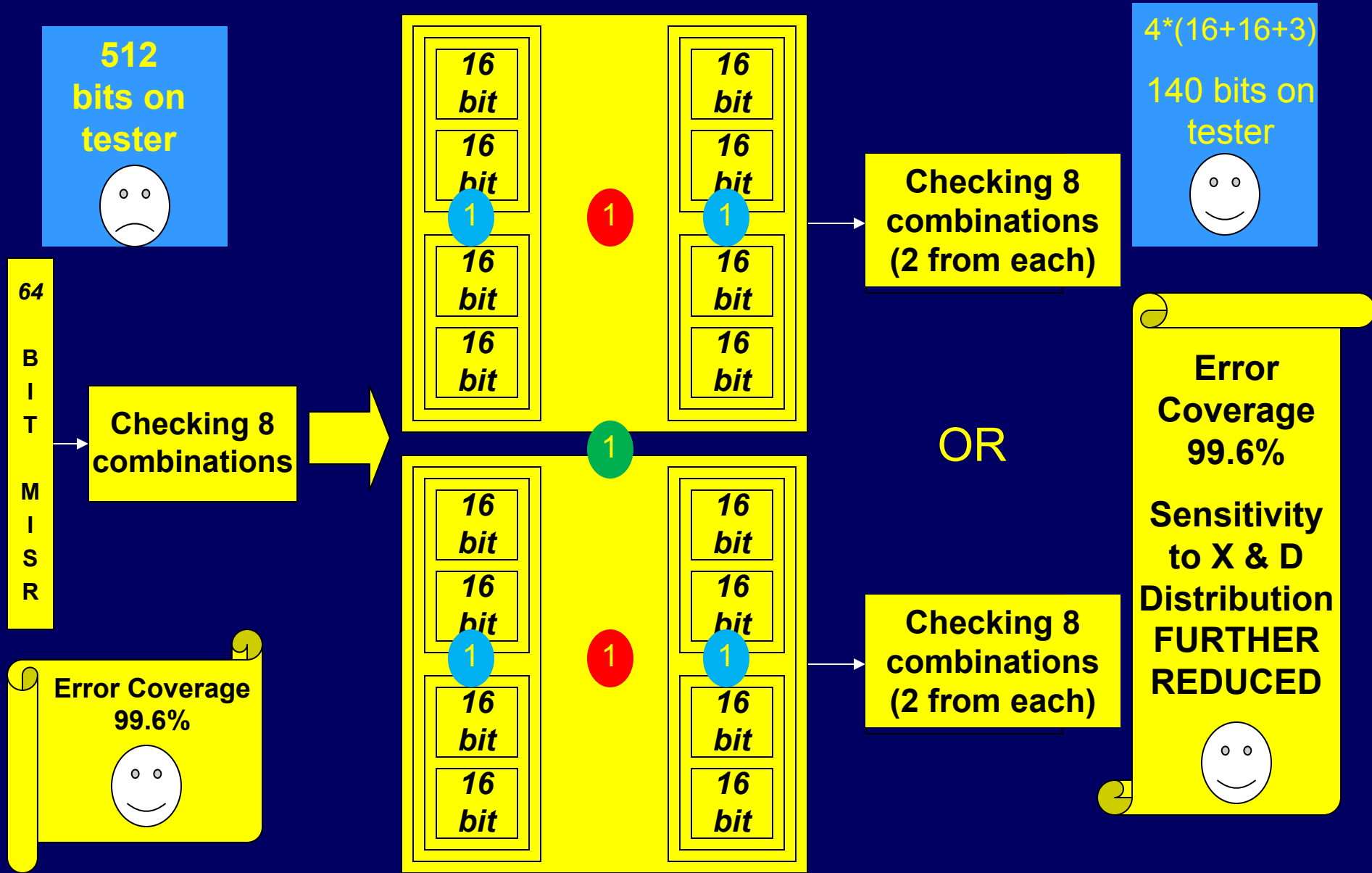
# DESIGN EXAMPLE





# DESIGN EXAMPLE



# DESIGN EXAMPLE



# COMPARISON

	Probabilistic Observation	Deterministically Targeting D's
<b>MISR Requirement</b>	1 64-bit MISR	16 16-bit MISRs
<b>Dependence on X's</b>	YES	YES
<b>Dependence on D's</b>	NO 	YES
<b>X's/D's Tolerated</b>	56	56
<b>Combinations checked</b>	8 (99.6% error cov.)	8 (99.6% error cov.)
<b>Bits on Tester</b>	$64 * 8 = 512$	$4 * (16 + 16 + 3) = 140$
<b># bits</b>	$512 / 56 = 9.2$ per X	$140 / 56 = 2.5$ per X or D 

# COMPRESSION ACHIEVED

% of X's	% of D's			
	1%	2%	4%	6%
1%	21.3x	14.5x	9.0x	6.6x
3%	11.0x	9.0x	6.6x	5.3x
5%	7.6x	6.6x	5.3x	4.5x
8%	5.3x	4.8x	4.2x	3.7x
10%	4.5x	4.2x	3.7x	3.3x

# COMBINING WITH X-MASKING

## Combining X-Canceling with X-Masking

- Do Not Need to Mask All X's
- Target Only Easy-to-Mask X's

## Do Not Need to Mask All Scan Chains or Scan Slices Containing X's

- If Masking X Blocks Observation of Fault
  - Let X Pass Through to X-Canceling MISR

# CONCLUSIONS

**Tester Storage Requirements  $O(\text{Total } X\text{'s})$**

- Independent of Scan Architecture

**Error Coverage Arbitrarily High**

- Independent of Distribution of  $X$ 's

**Area Overhead**

- Linear in Size of MISR

**For X-Bounding**

- Can Use as Safety Feature – Handle Unexpected  $X$ 's