



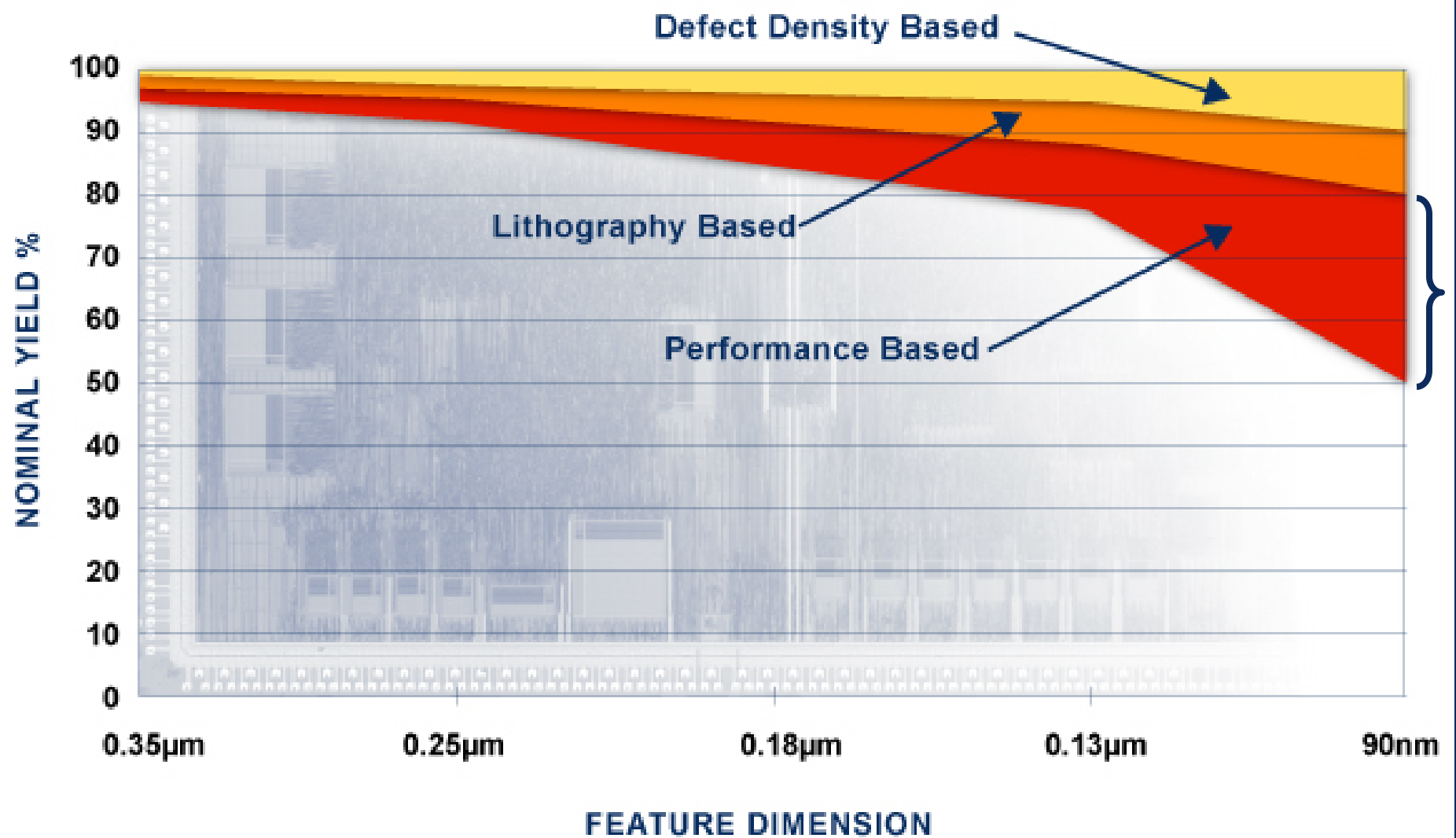
BIST Techniques for Delay and Jitter in Nanometer Technology ICs

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Southwest DFT Conference

May, 2007

Importance of parametric tests



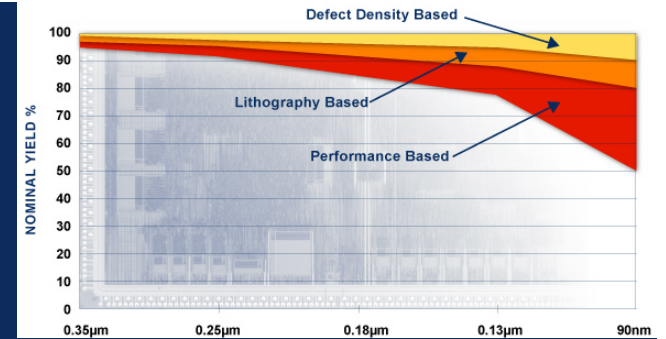
Introduction

Importance of parametric tests

- 30% yield loss in 90 nm ICs
- Increased sensitivity to V_{DD} (due to lower V_{DD})
- Increasing portion of logic paths are critically timed
- Higher on-chip clock rates, use of PLLs, DLLs, SerDes

Test problems

- Decreasing test access – pins, signal integrity
- Digital circuits (incl. DFT) becoming more analog
- PLL, DLL, SerDes: mixed-signal test



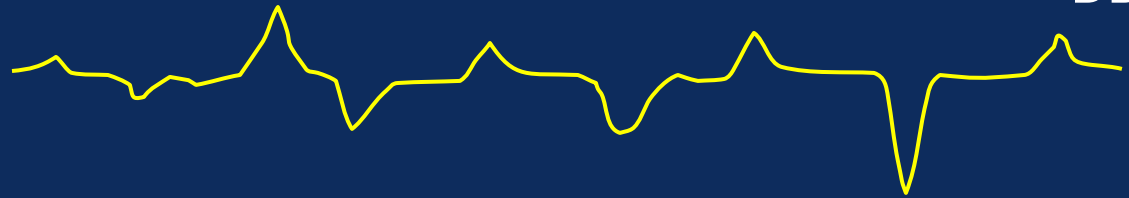
At-speed logic BIST

Structurally tests all logic functions at rated speed

- i.e. all logic path delays less than 1 or 2 clock periods
- Including asynchronous clock domains

Must manage steady-state and instantaneous V_{DD}

- Analog!

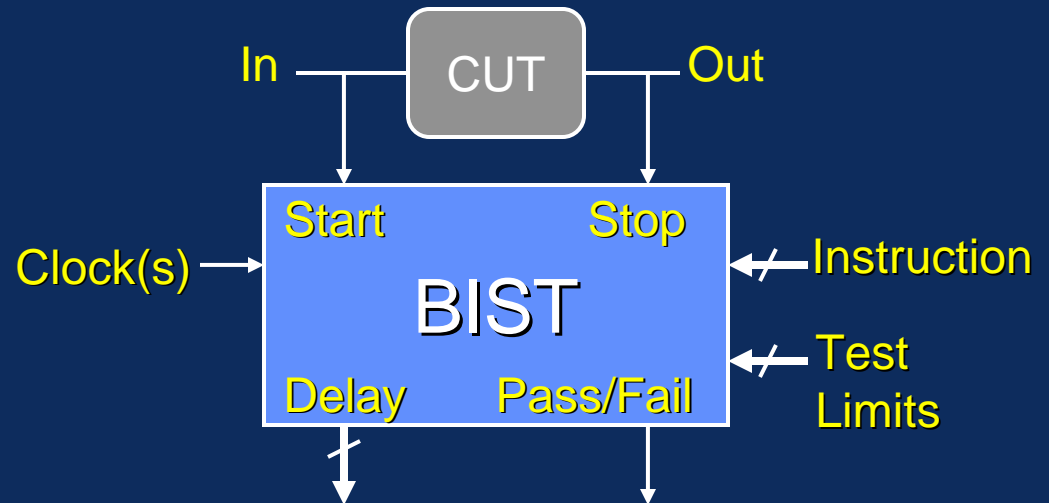


Not discussed in this presentation

Outline

BIST techniques that measure delays and jitter

- Charging a capacitor
- Counter
- Delay lines (3 types)
- Ring oscillators
- Undersampling



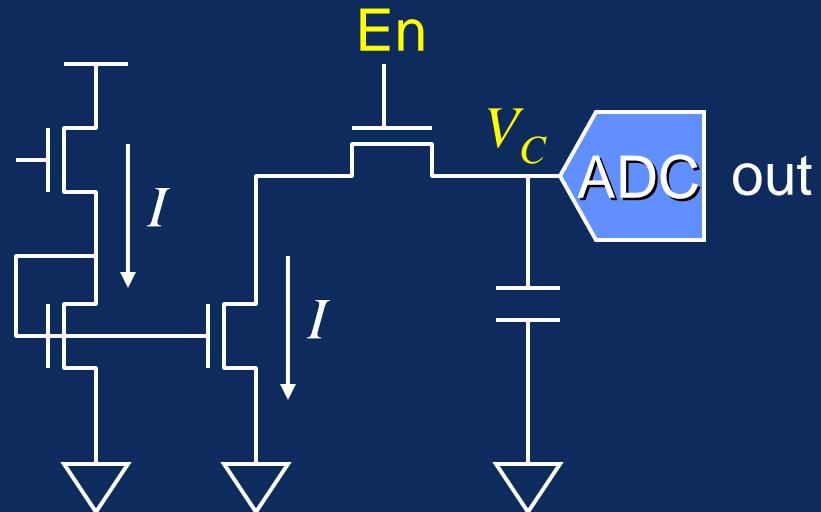
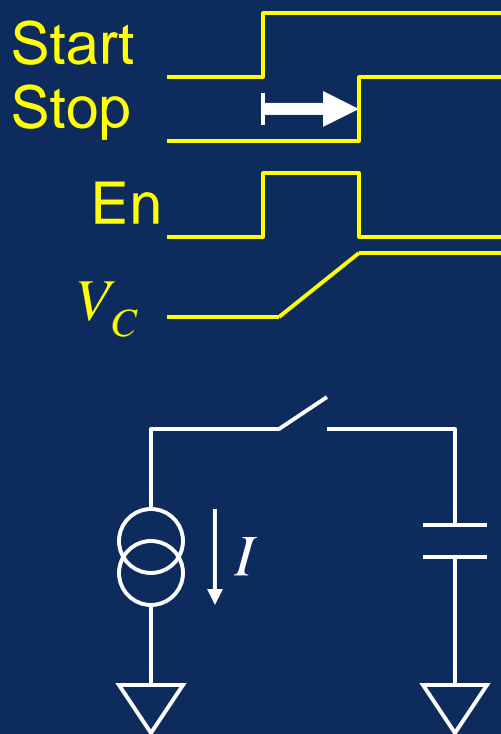
Conclusions

- Simplest, most common, highest performance

Charging a capacitor

Principle of operation

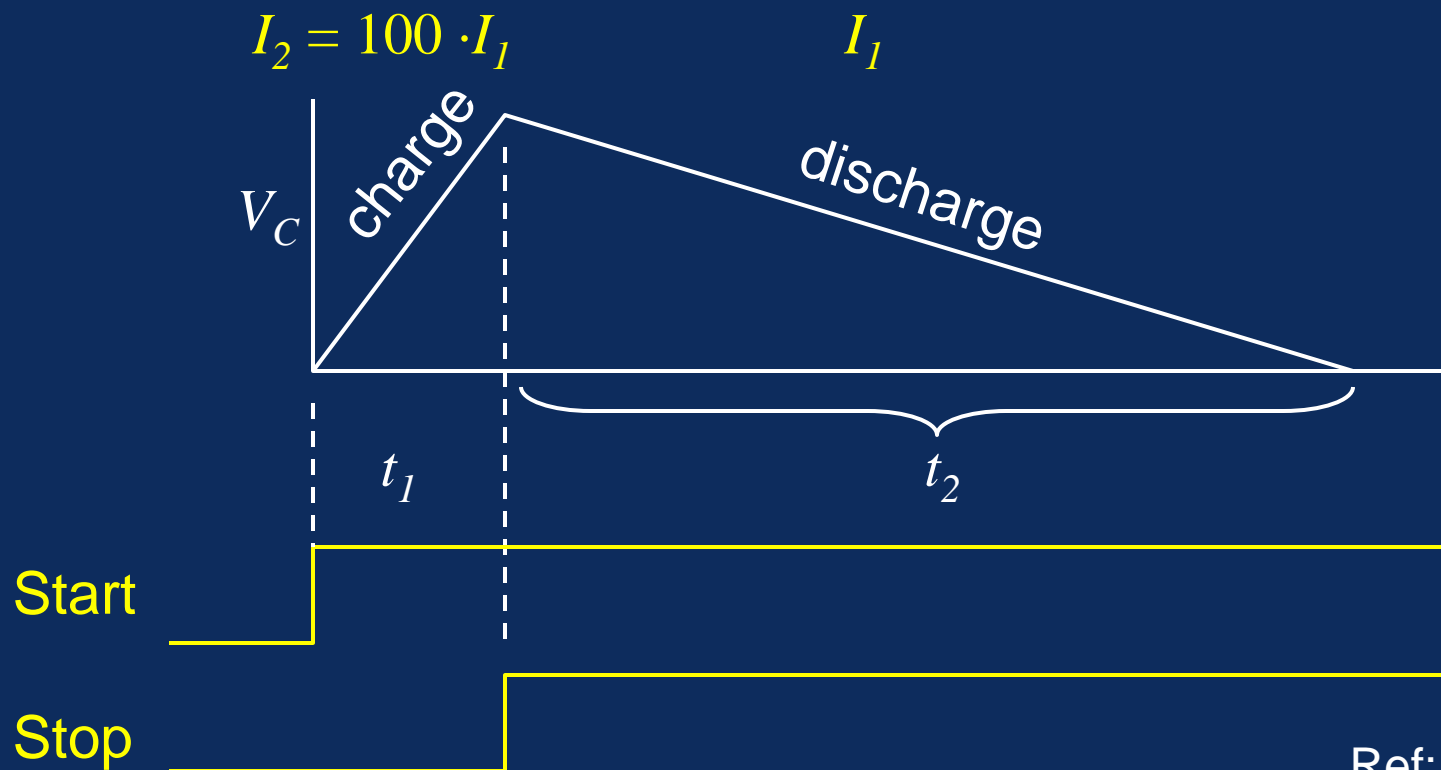
- Constant current charges capacitor for time interval
- Convert capacitor's voltage to digital value



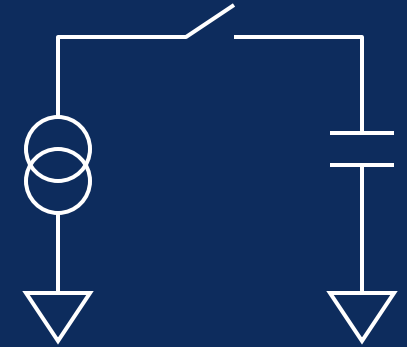
Charging a capacitor

Improvement

- Dual slope integration – avoids use of ADC
- $t_1 = t_2 \cdot I_1/I_2$



Charging a capacitor



Advantages

- 'No' minimum pulse width or resolution

Disadvantages

- Analog – sensitive to process and noise, or complex
- ADC or current multiplier – how tested?

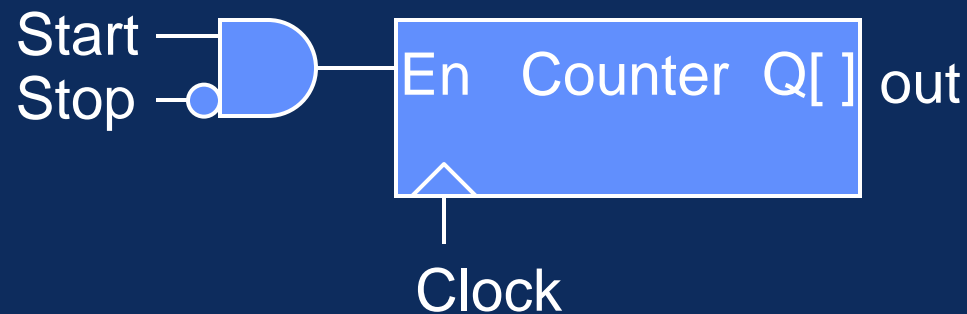
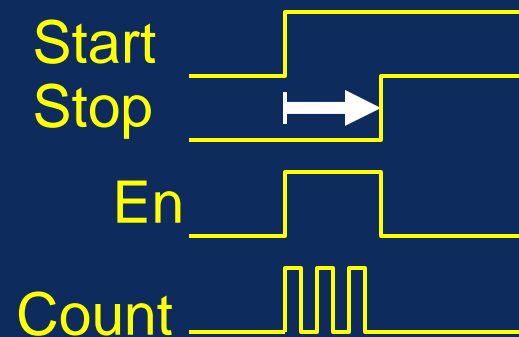
Performance

- 10 ps resolution (simulation)

Digital counter

Principle of operation

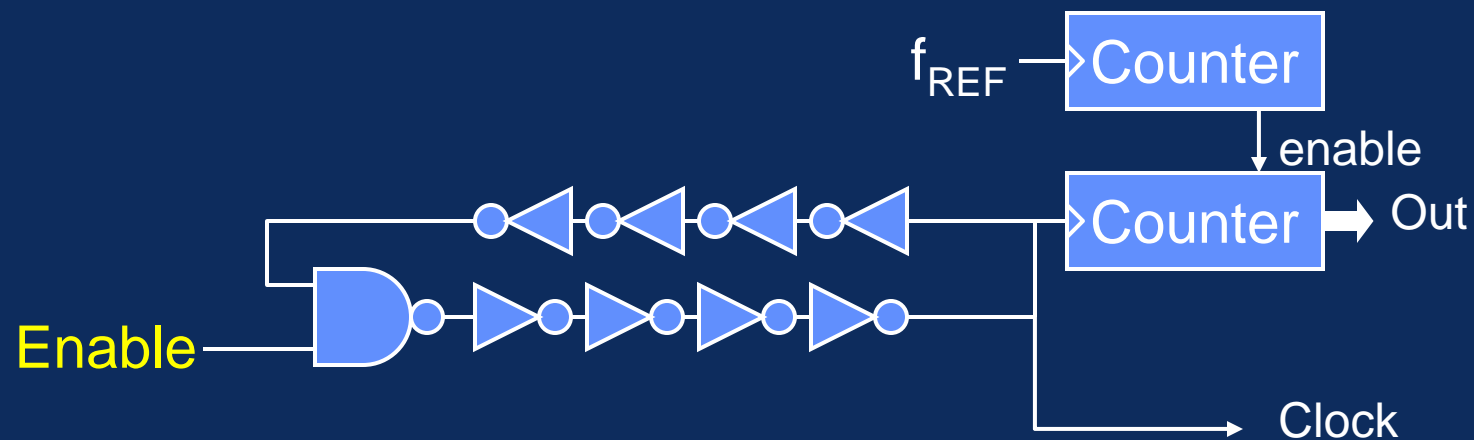
- Count clock pulses for time interval



Digital counter

Improvement

- On-chip ring oscillator as clock source
- Measure oscillation frequency with frequency counter



Digital counter



Advantages

- Digital – process insensitive, RTL→layout, scan test
- Linear, with ‘unlimited’ range

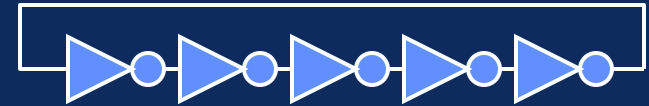
Disadvantages

- Minimum pulse width is one clock period
- Power & noise if HF clock specially created

Performance

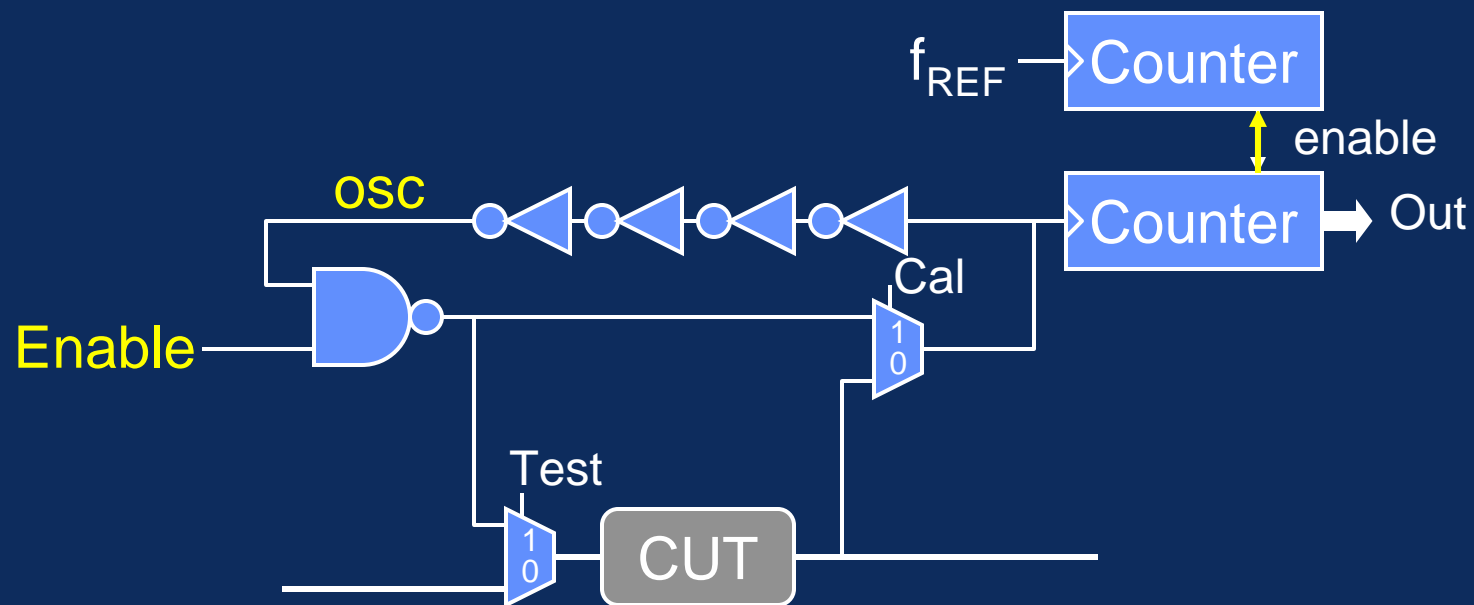
- One period of 0.1~10 GHz clock (>100 ps)

Ring oscillator

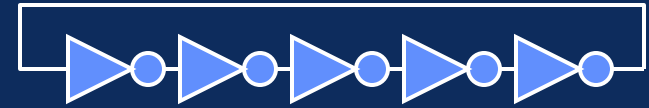


Principle of operation

- Selectably include CUT in ring oscillator
- Measure difference in oscillation frequency (period)



Ring oscillator



Advantages

- Same as digital counter
- Infinite resolution (given enough time)

Disadvantages

- Must insert multiplexer at CUT input (adds delay)
- Can't measure CUT in mission mode (on-line)

Performance

- Picosecond resolution (mux limits accuracy)

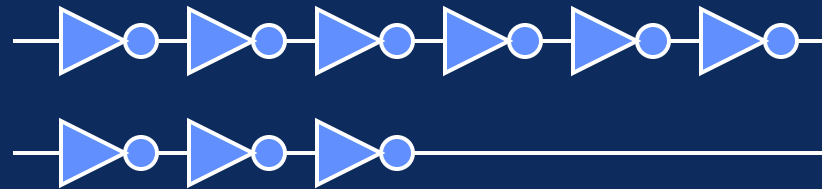
Delay lines

One delay line



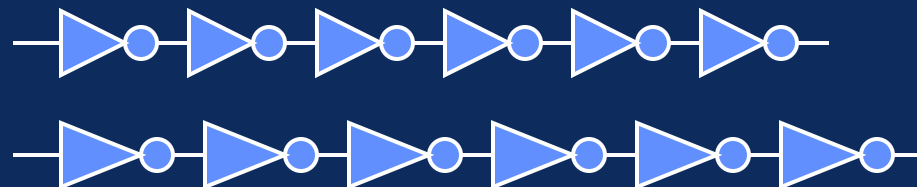
- Compare time interval to taps of delay line

Two delay lines



- Add constant delay to one of the two signals
- Measure positive and negative delays

Vernier delay lines

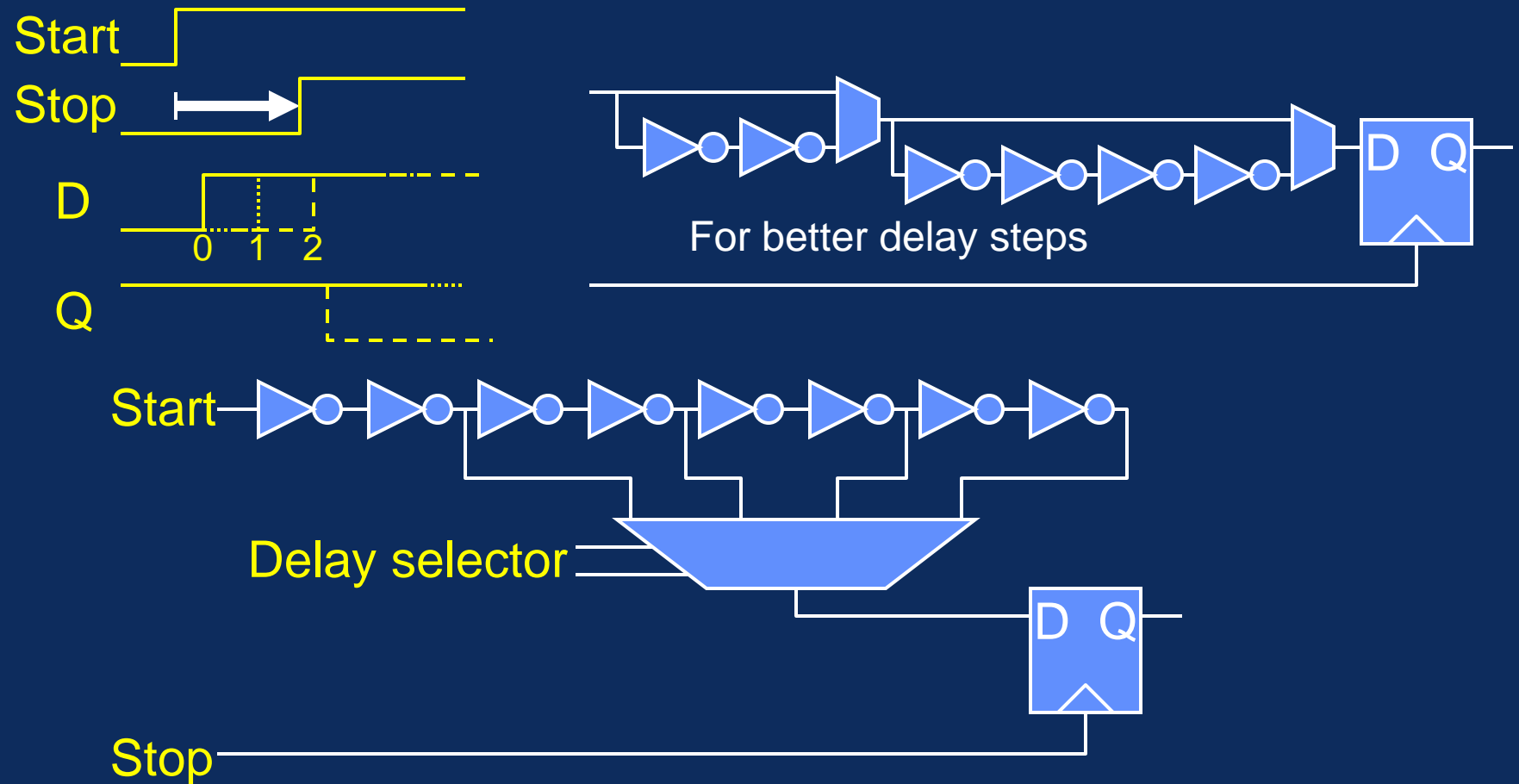


- Different gate delays in each line
- Finer time resolution

One delay line

Principle of operation

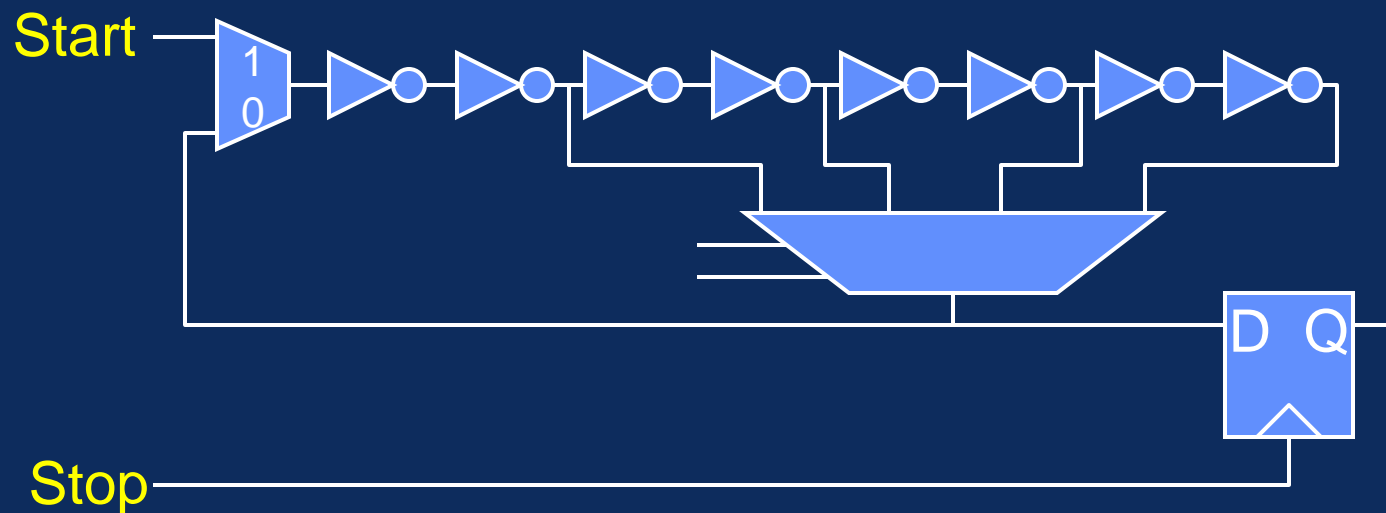
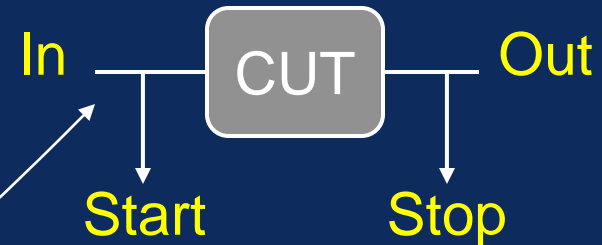
- Compare time interval to delay line: selector setting



One delay line

Improvement (a)

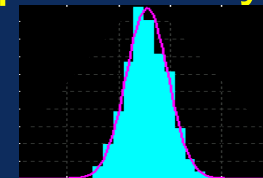
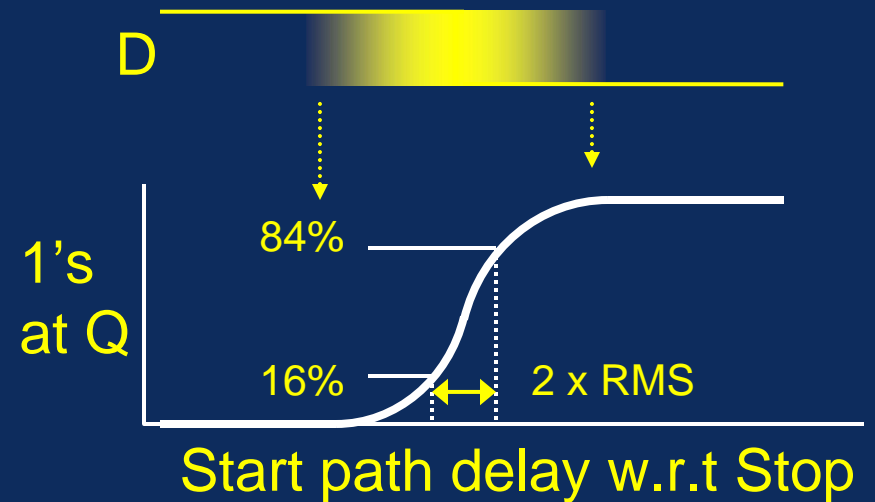
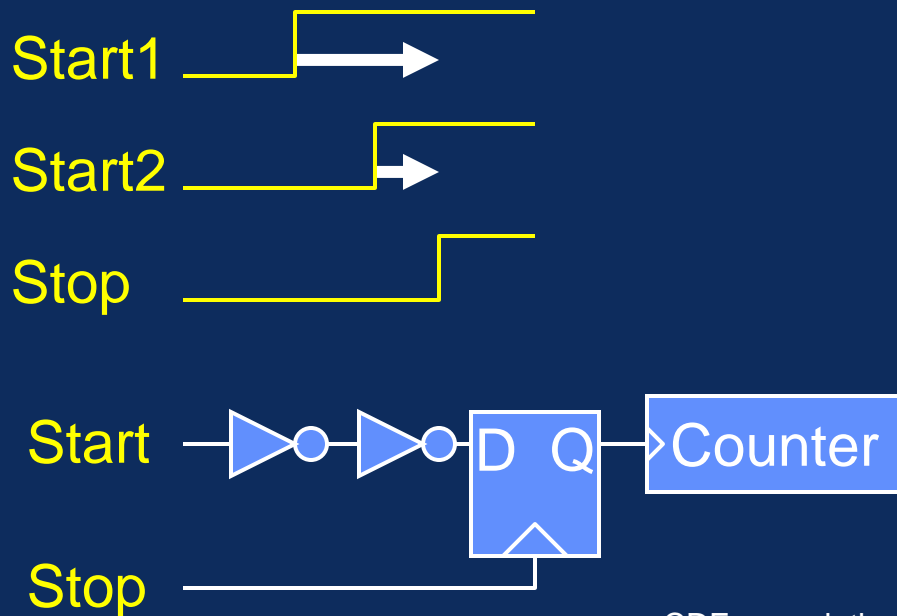
- Self-jitter
 - Differential logic
 - Low jitter input signal



One delay line

Improvement (b)

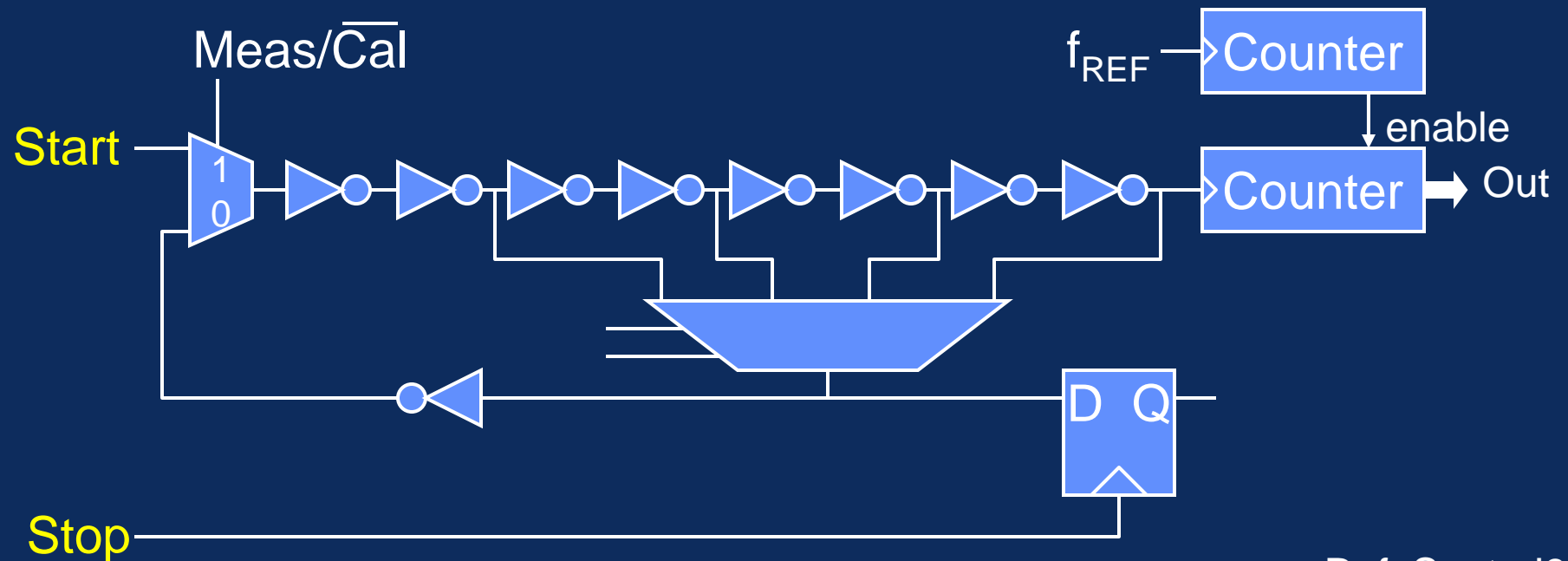
- Only measure delay differences
 - Unknown, constant delay errors will cancel
 - Can measure CDF of *random* jitter to estimate RMS value by adjusting delay to get target % 1's



One delay line

Improvement (c)

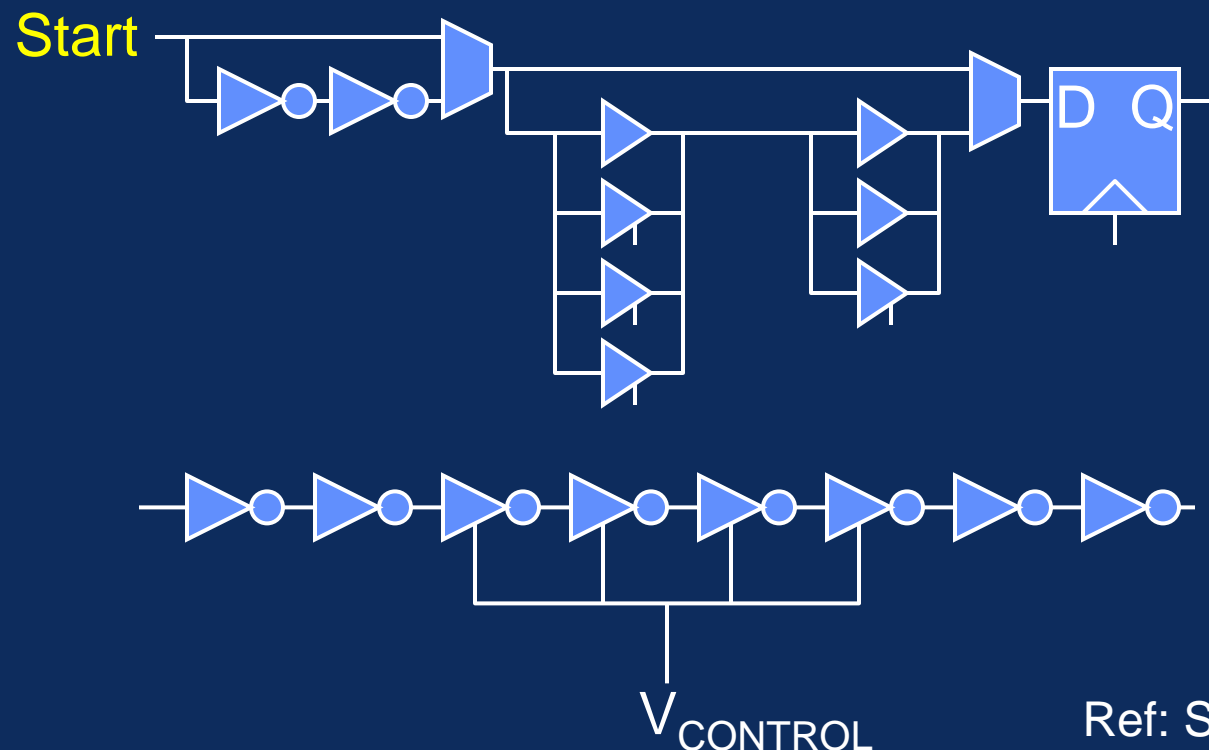
- Calibration
 - Convert into a ring oscillator, measure oscillation period
 - Best accuracy when measuring changes in delay



One delay line

Improvement (d)

- Finer resolution
 - Digital: $\sim 1/8$ gate delay or ~ 4 ps (with shared power rail)
 - Analog: < 0.5 ps (differential, calibration, quiet power, V_C)



One delay line



Advantages

- Mostly digital – auto RTL → layout (maybe)

Disadvantages

- Process and power rail sensitive
- Limited delay range (and jitter proportional to delay)
 - Requires more inverters (hundreds) in faster technologies
 - Sets low frequency limit for clock period measurement

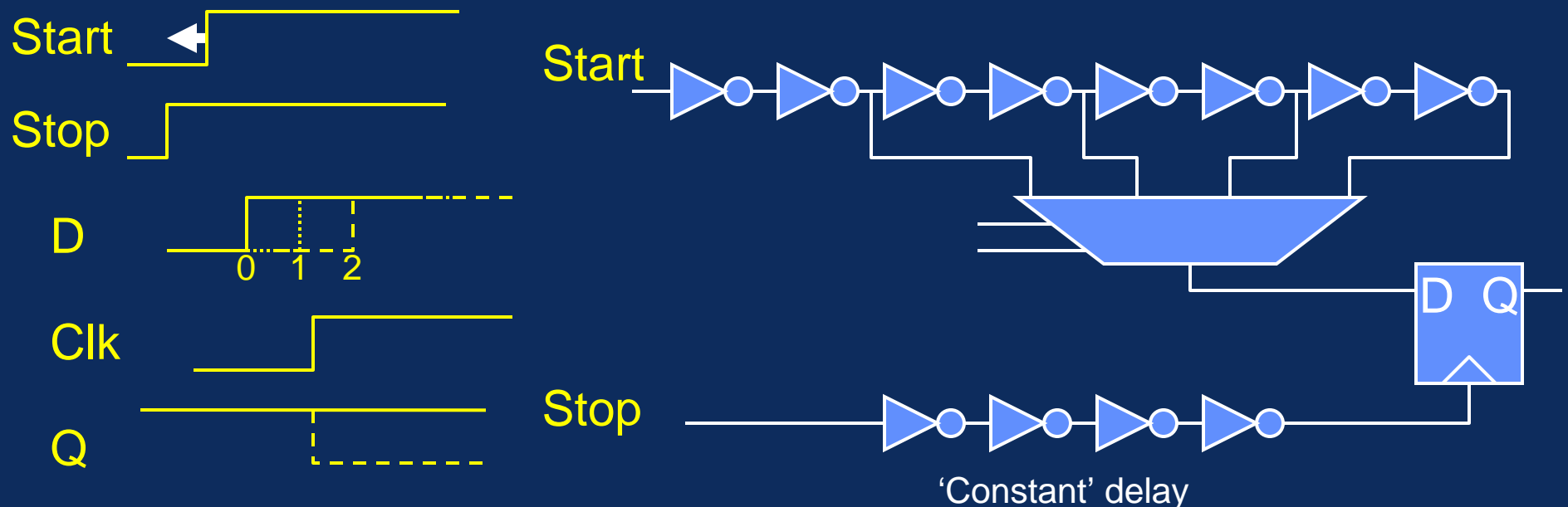
Performance

- >50 ps for single measurements, <10 ps for differences

Two delay lines

Principle of operation

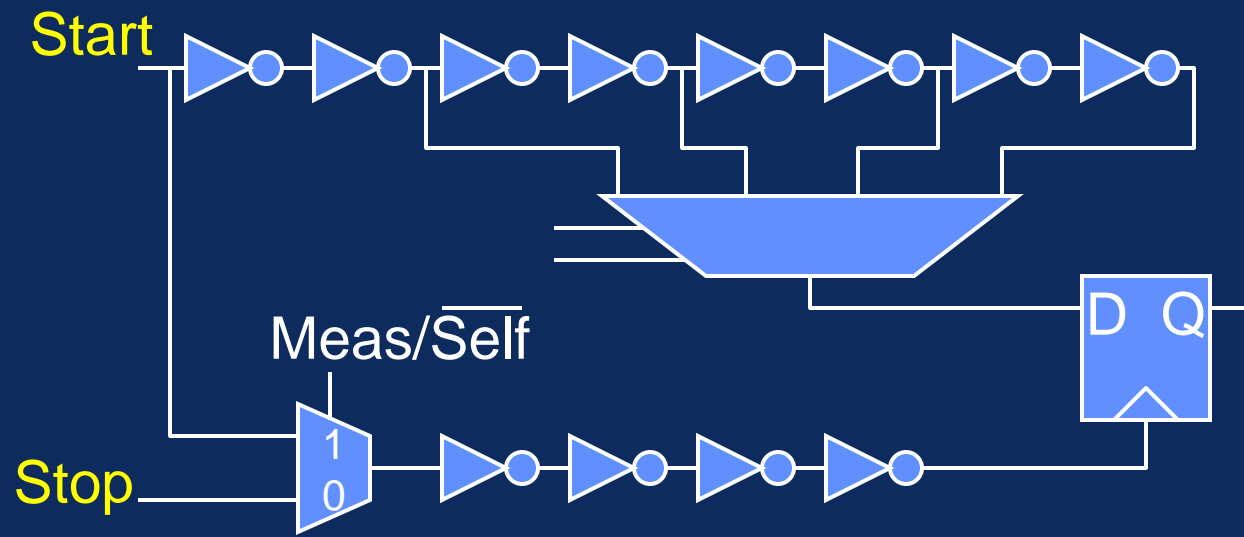
- Add a constant delay (half first delay) to second signal
- Measure \pm delays, magnitude $<$ constant delay



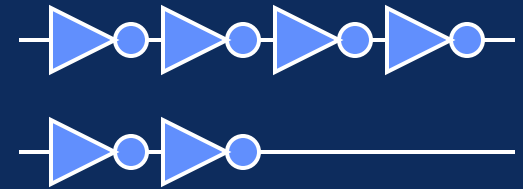
Two delay lines

Improvements

- Self-test jitter of the delay lines
 - Measure jitter in one delay line, using the other
 - Does not measure correlated jitter



Two delay lines



Advantages

- Measures positive/negative delays (if unknown *a priori*)
- Can measure self-jitter
- Same as one delay line

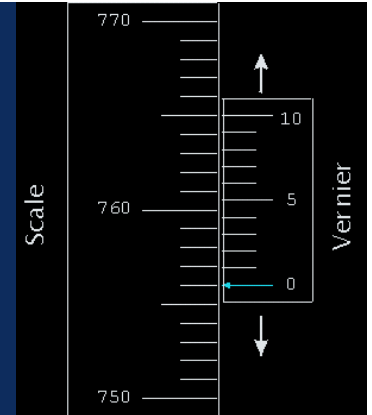
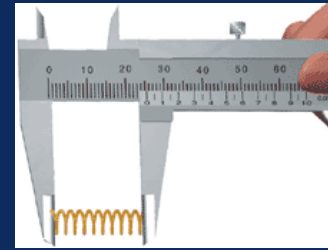
Disadvantages

- Same as one delay line, plus more delay step variation
- Both delay lines contribute jitter to measurement

Performance

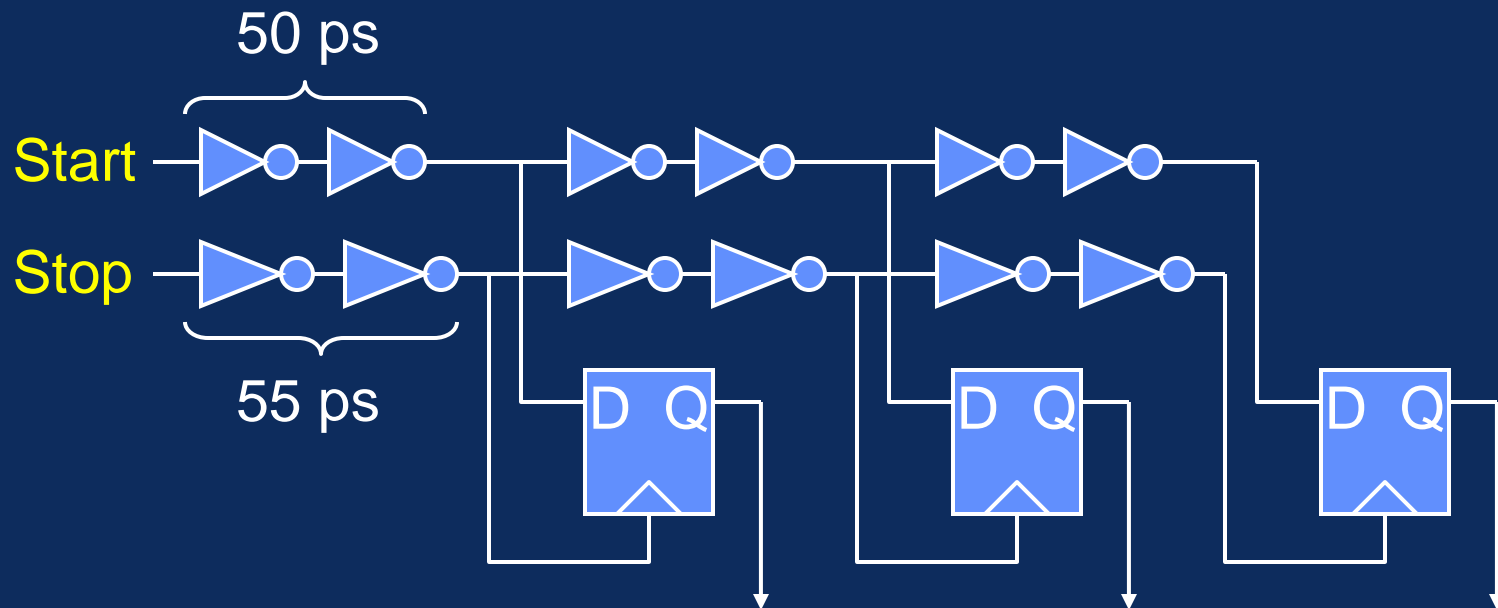
- <1 ps with careful layout, >10 ps without, 0.1~ 2 GHz

Vernier delay lines

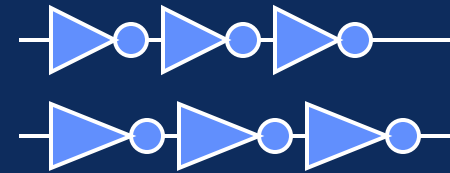


Principle of operation

- Delay increments of second line are slightly longer
- Resolution equal to difference in increments



Vernier delay lines



Advantages

- Mostly digital – RTL → layout (maybe)
- More systematic layout than other delay approaches

Disadvantages

- Same as two delay lines, but more layout-sensitive

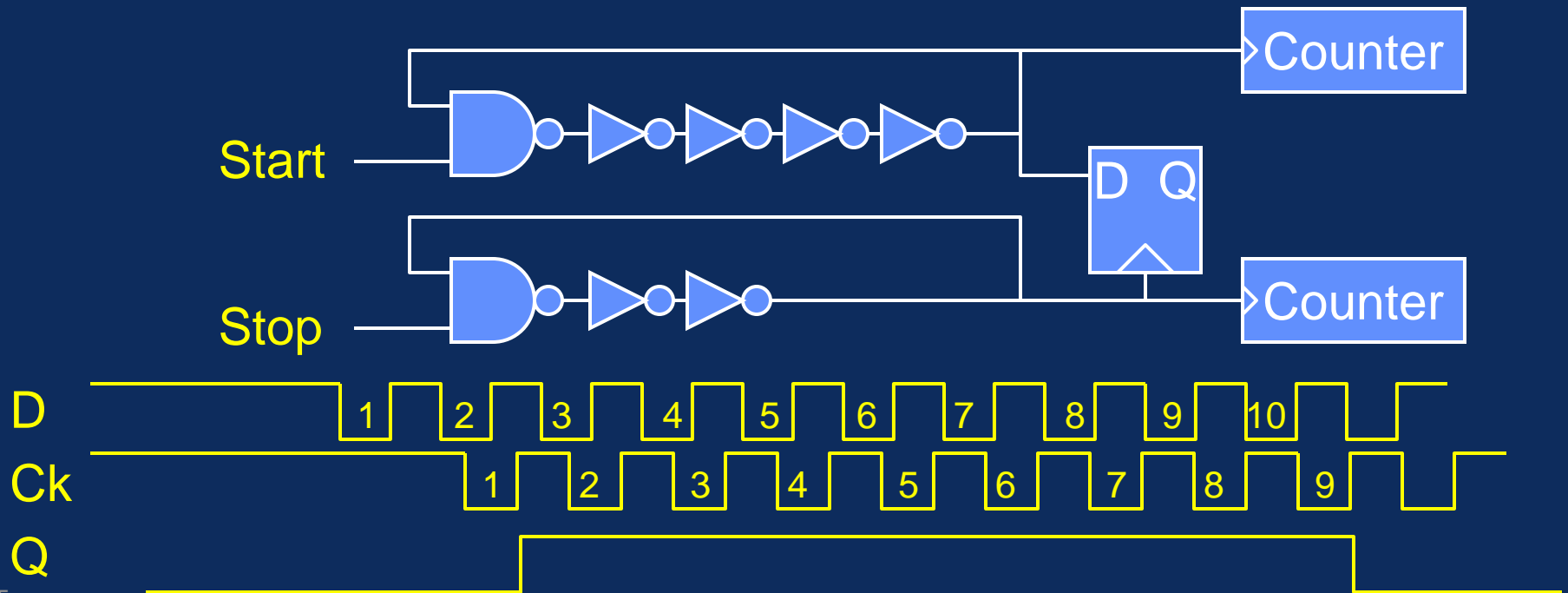
Performance

- Better than two delay lines
- Sub-picosecond resolution if careful layout

Vernier ring oscillators

Principle of operation

- Two gated ring oscillators, with slightly different freq.
 - Measure using frequency counters
- Count both oscillations until their edges align



Vernier ring oscillators

Advantages

- Same as Vernier delay lines, but 'unlimited' delay range
- Fewer inverters, so feasible to use differential gates

Disadvantages

- Same as Vernier delay lines, but more complex
- Jitter accumulates in ring for duration of osc. counting

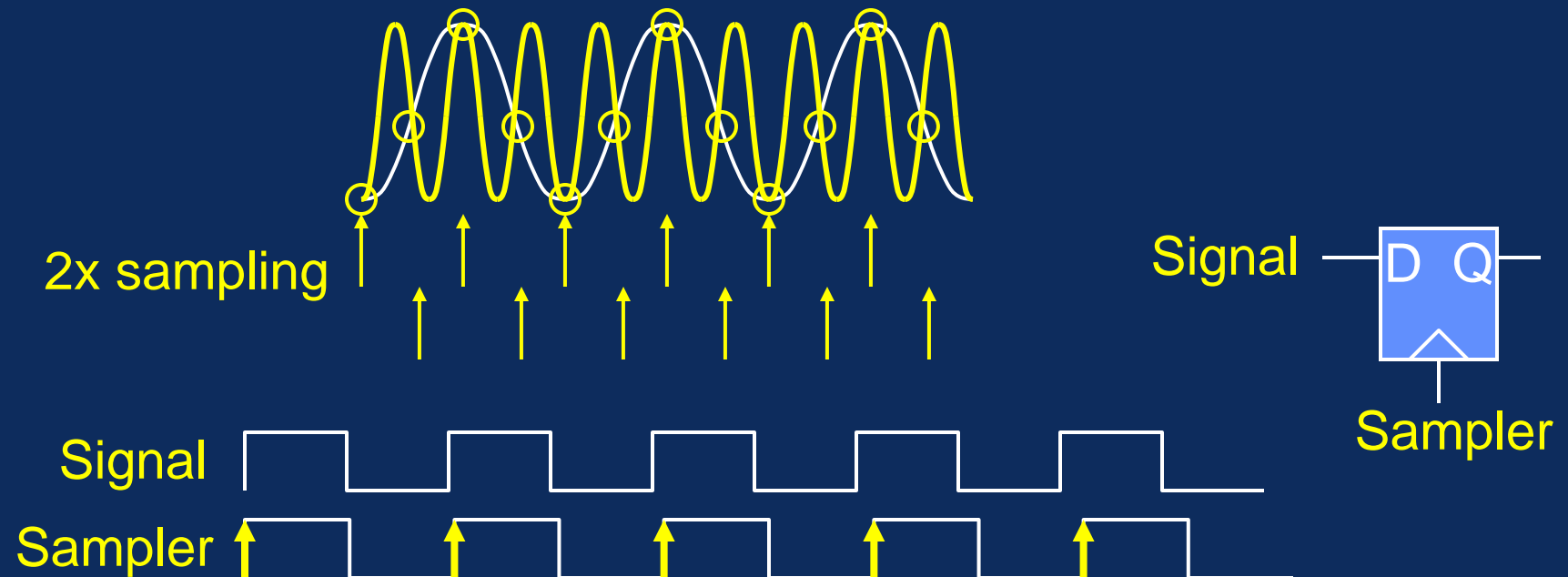
Performance

- 10 ps ("1 ps" on stand-alone test chip)
 - Oscillators might phase lock to each other with smaller values

Undersampling

Principle of operation

- Nyquist criterion: Sampling a signal at $>2x$ highest freq. permits complete reconstruction
- Sampling at $<2x$ is “undersampling”, causes aliasing

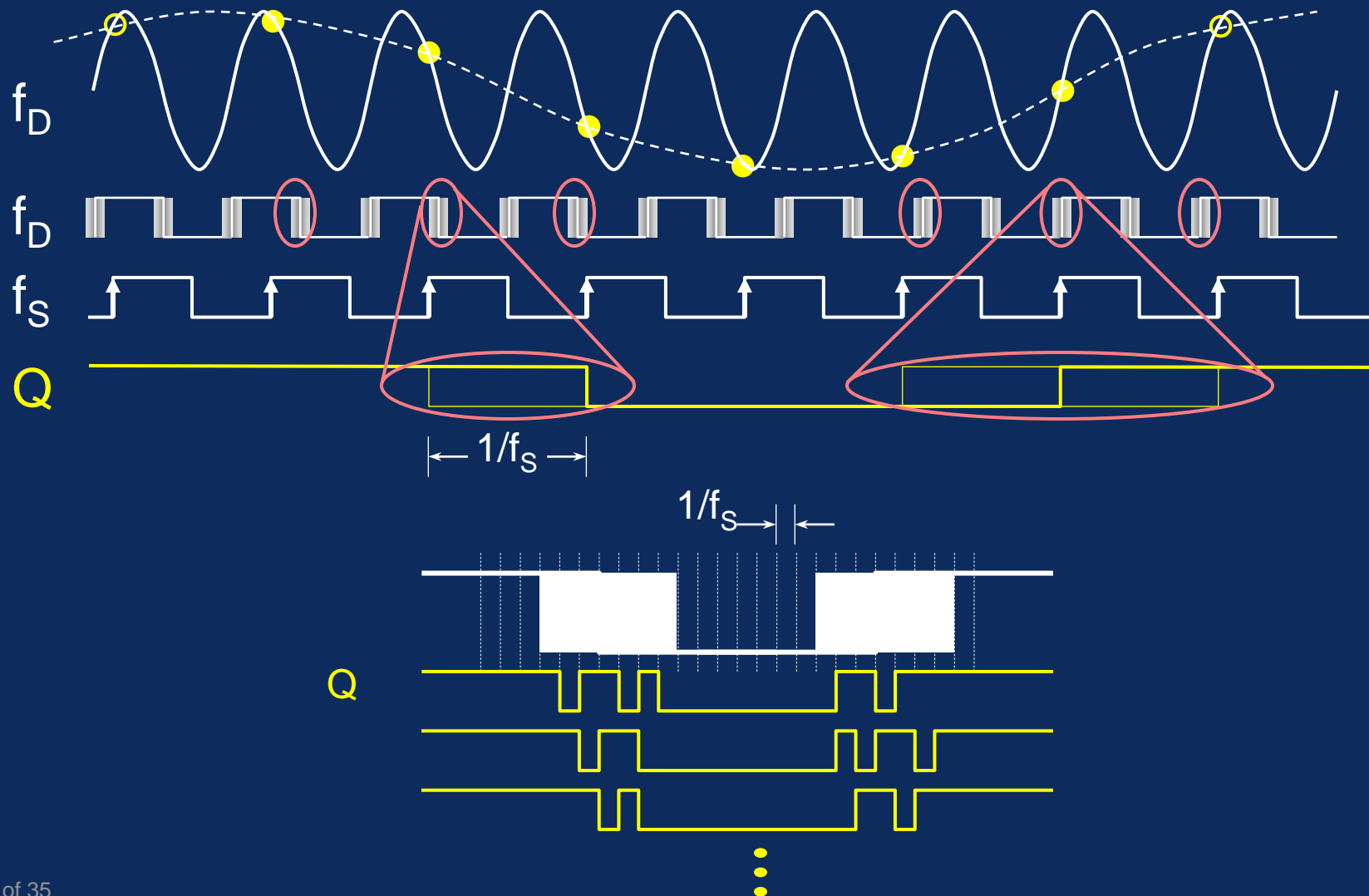


Undersampling

Signal
 f_D



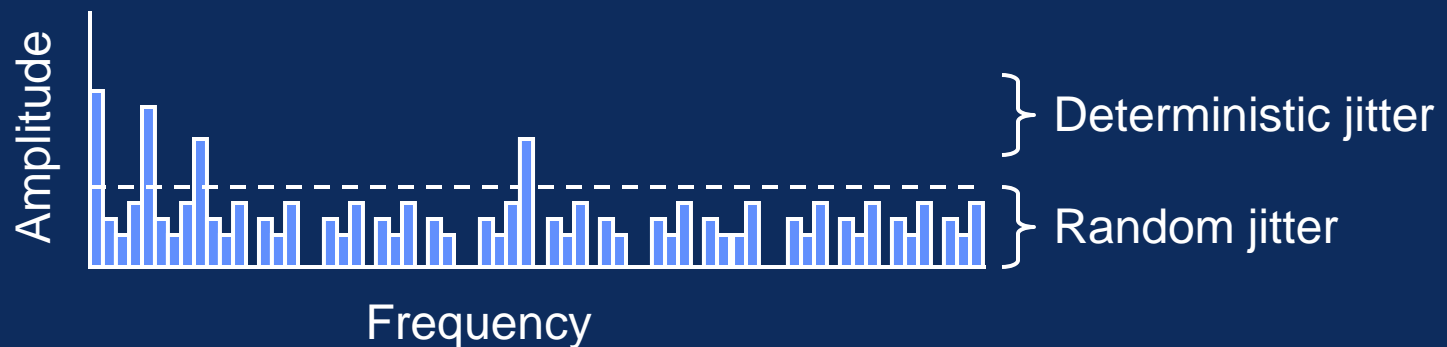
Sampling
Clock
 f_S



Undersampling

Analysis

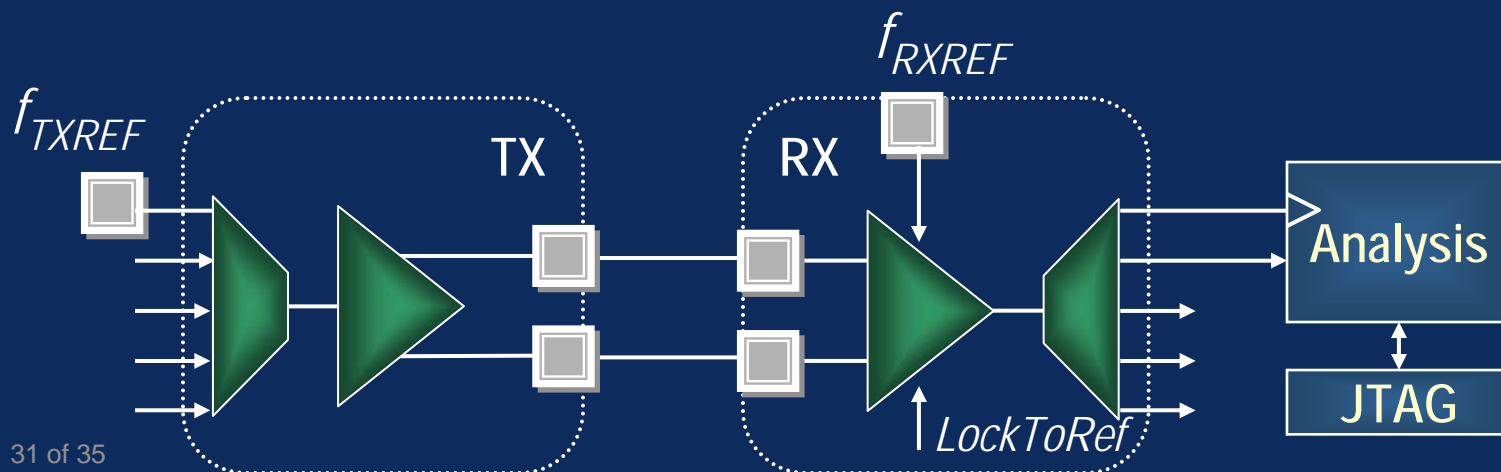
- Count sampling clock cycles in expanded waveform
 - Use digital counter technique to measure time delays
 - Sampling resolution must be coarser than pk-pk jitter
- Fourier transform
 - Mathematically convert sample values to frequency domain
 - May require >1 million samples, long computation time
 - Separately measure random jitter and periodic signals



Undersampling

Improvement (a)

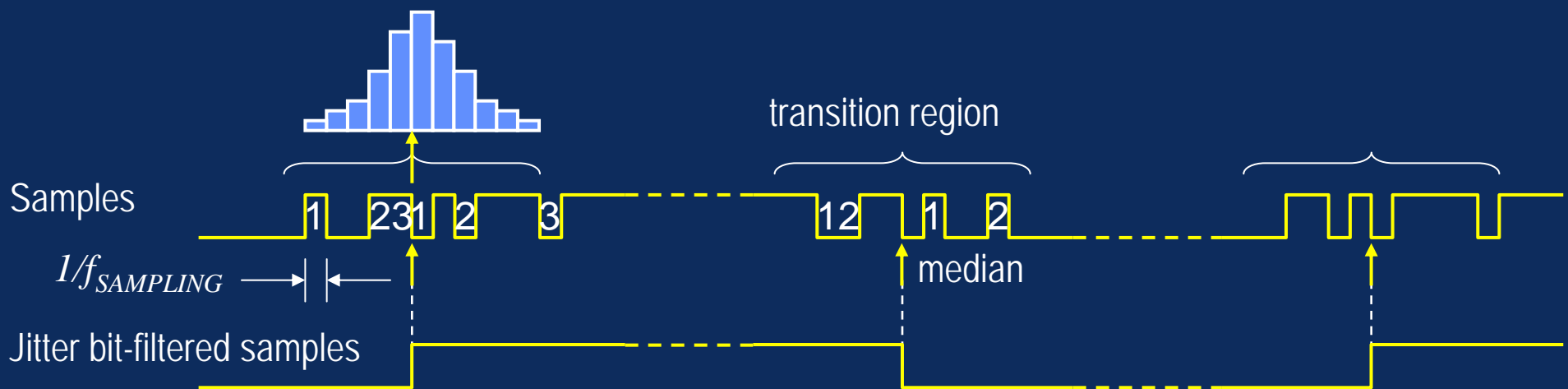
- Sampling latch
 - Differential
 - Reduce effects of power rail noise and impact on CUT
 - High bandwidth
 - For sampling multi-GHz signals
 - Use CUT (SerDes receiver)
 - So that sampler's jitter is intentionally in measurement



Undersampling

Improvement (b)

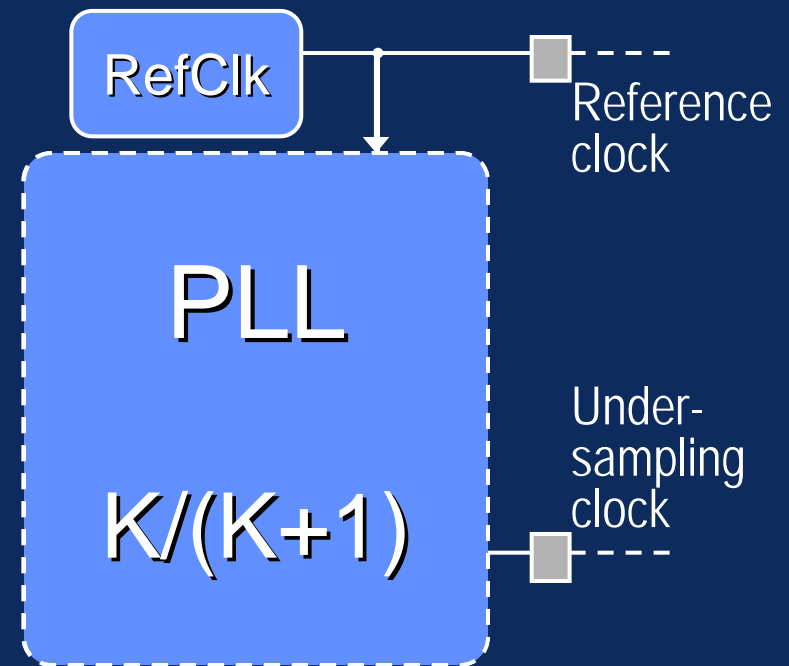
- Analysis
 - Measure CDF or histogram of jitter, and estimate RMS on-chip
 - Separately measure HF and LF jitter
 - Jitter bits caused by HF jitter; median wander caused by LF jitter
 - Cutoff frequency: $f_J = W \cdot f_{OFFSET} / (2\pi A_J)$



Undersampling

Improvement (c)

- Sampling clock
 - Differential input pins
 - Low-jitter source
 - Crystal oscillator or VCXO
 - Telecom quality PLL IC
 - Laboratory clock generator
 - Precise frequency offset
 - Eliminates effects of low frequency jitter in clock sources
 - PLL clock source



Undersampling

Advantages

- Minimal process sensitivity, no calibration
- 'Unlimited' range, adjustable post-silicon

Disadvantages

- Requires a sampling clock
- May require loadboard sampling clock generator
 - For precision frequency, and low jitter

Performance

- <0.5 ps to >1 μ s: best BIST in real silicon, by $>10X$
 - Controlled by frequency offset (difference in clock periods)

Conclusions → digital

Simplest delay measure

- Digital counter: Coarse resolution

Most common delay measure

- Ring oscillator: Infinite resolution, can't use for clocks, and adds mux to CUT

Simplest jitter measure, and most common

- Two delay lines: Fast, accurate, but limited range and noise sensitive

Highest performance delay and jitter measure

- Undersampling: Fast, accurate, unlimited range, but requires sampling clock

Related LogicVision® Products

ETPLL *(first customer silicon in 1999)*

- RTL-based BIST for PLLs with $f_{OUT} = 100 \text{ MHz} \sim 1 \text{ GHz}$
- Measures timing and period jitter to 5 ps rms, open loop gain, lock range, lock time
- Uses PLL's reference clock, and two delay lines

ETSerdes *(first customer silicon in 2006)*

- RTL-based BIST for SerDes, PLLs, DLLs with any f_{OUT}
- Measures jitter components (RJ, TJ, DCD, ISI, HF/LF) to 0.5 ps rms, phase errors, duty cycle, frequency
- Uses undersampling, and second reference clock

References

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