SiP – Catalyst for Innovation

SWDFT Conference
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ASE Group

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Outline

• Consumer Electronic Market
  > Consumer Electronics Market Trends
  > SiP Drives Innovation
  > SiP Category

• SiP - Challenges
  > Definition
  > Technologies & Infrastructure
  > Innovations

• Current Practice
  > Known Good Die
  > Production flows
  > Test Platforms

• The next wave in SiP
  > Collaborative Co-Design
  > Working outside the Box
The Consumer Electronics Market
2006 Semiconductor Market
Source: SIA 2006

2006 $250B / +9.8%

- Consumer 17.2%
- Automotive 8.7%
- Wired Comm 7.0%
- Industrial/Military, 7.3%
- PC/Computer 43.7%
- Cell Phone/mobil, 17.0%
- Wired Comm 7.0%
- Digital TV Shipment +52% (units)
- Camera Shipment +16% (units)
- MP3 Shipment +52% (units)
- PC Shipment +10~12% (units)
- Cell Phone Shipment +20% (units)
Consumer Market Imperatives ...

Source: ITRS Conference, 2005 July
Consumer Markets Are Becoming Dominant

- Previously driven by Corporate and military requirements
- "Tricky" Markets
  - Fashion-driven and price sensitive
  - Cool and trendy is hard to define and harder to deliver
  - New Brands & New Players
- High-volume but fragmented applications
- 3 I’s - Innovation, innovation, innovation
  - Market
  - Products
  - Technology

Source: Gartner Dataquest Estimates (August 2006)
Consumer-Driven Market: Faster Product/Technology/Development

Cost of Delay
1. Lost Sales
2. Increased Expense
3. Opportunity Cost

Current Product
- Development Time
- Slippage
- 12- to 18 Month Product Life Cycle

New Product
- Development Time
- 4- to 10-Month Product Life Cycle
Innovations
A few Examples

Manufacturing
> Wafer thinning
> Wirebond
> Materials: Molding Compounds, DB Epoxy & films....
> Wirebond - flip chip Hybrids
> Substrates

Package Architecture
> Stacked dies, PoP, PiP, TSV, ......

Design & Test
> Co-design tools & environments
> Test methodologies
> Integration of process technologies (RF, analog/mix signal, and Digital)

And Many More
SiP - Situation Today

- **Markets:** End User Markets are the driver for SiP. Consumer Electronics, principally cell phone, demand diverse functions, size, time to market, and cost, & set in the momentum. Now applications in laptops, networks, automotive, medical, industrial applications have followed.

- **Volume Growth:** In 2006, 3.31 Billion SiPs were assembled. By 2010, this number is expected to reach 5.95 Billion,* growing at an average rate of about 16% per year.

- **Technology:** SiP applications have become the technology driver for small components, packaging, assembly processes and for high density substrates. New variants of SiP technologies are fast proliferating. 3D packaging and TSV technologies are leading the way.

- **SiP vs SoC:** Not the question

*Source Techsearch International 5-2007*
System-in Package (SiP) definition

SiP definition is:

“System in Package (SiP) is a combination of multiple active electronic components of different functionality, assembled into a single unit, that provides multiple functions associated with a system or sub-system. An SiP may optionally contain passives, MEMS, optical components and other packages and devices.”

International Technology Roadmap for Semiconductors 2006
### Categories of SiP

<table>
<thead>
<tr>
<th>Horizontal Placement</th>
<th>Wire Bonding Type</th>
<th>Flip Chip Type</th>
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</thead>
<tbody>
<tr>
<td><strong>Stacked Structure</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interposer Type</td>
<td>Wire Bonding Type</td>
<td>Wire Bonding + Flip Chip Type</td>
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<tr>
<td>Interposer-less Type</td>
<td></td>
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<tr>
<td><strong>Embedded Structure</strong></td>
<td>Chip(WLP) Embedded + Chip on Surface Type</td>
<td>3D Chip Embedded Type</td>
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<td></td>
<td>WLP Embedded + Chip on Surface Type</td>
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</tbody>
</table>

Source: ITRS 2006 - 20030710 K. Nishi, Hitachi, JEITA, Revised by H. Utsunomiya
SiP Challenges
KEY SiP CHALLENGES

Die Co-Design

Cost Analysis

Design Tool Linkage

Package DFM

Substrate DFM

Design For Test

Modeling & Simulation

Package Co-Design
• Major Roadblocks

> Lack of tools for Chip-Package Co-Design
  » Dies – Package – Substrate
  » Physical simulations – electrical, thermal, mechanical,
> How to test chips & package
  » DFT, package test, KGD strategies
> How to integrate and test different type of memories
  » Alternative design & package options
  » Debug & yield enhancements
> How to implement 3D SiP technologies, e.g. TSV
COLLABORATIONS

• Collaborations Between All Parties in The Supply Chain is Crucial
• EDA Tools to Address The 3D Environment Inside SiP, Predictable Designs is Required
• DFT Strategy and Plan During IC and Substrate Design Phases is Critical for Debug and Yield Enhancements
• Memory Vendor to Supply Standard Form Factor and Test Methodology
Current Practice
• KGD Solutions
  > Characterize individual die
  > Wafer sort with final-test (FT) quality
    » At-speed wafer-probing
    » Comprehensive DFT for KGD testing at low speed
  > Package-level burn-in conducted through WLBI

• Design for “Connectivity Test” at FT
  > DFT for failure analysis
  > Multi test platform, multi insertion test flow
SiP Test Flow

Top Package
- Memory 1 Wafer Received (KGD)
- Memory Assembly
- Test (Burn In)
- Test (Final Test)
- Memory (Known-Good-Package)

Middle Package
- Memory Assembly
- Memory B/I
- Memory FT

Bottom Package
- ASIC Wafer Received
- Wafer Probe
- IC Package assembly
- Package Final Test
- ASIC (Known-Good-Package)

Assembly

PKG Stacking

SIP Final Test

Test

Shipping
Test challenges for SiP

- Accessibility
- Controllability
- Observability
- Failure Localization, Failure Analysis
- Deep Memory and Mixed Signal
- Test Time Explode due to Memory Test
- Design for Test (DFT)
Memory Test Strategy for SiP

“Cost is King”

Separate memory Insertion
OR
One memory + SOC insertion

Device mix,
Package type,
Accessibility

How much capacity
Needed
SOC, Memory

“Yield is God”

Memories in the SIPs
Pin counts, volumes, mix
Test times, site counts
Considerations of SiP Memory Testing

Wafer & final testing requirement
- Laser repair
- Test time (10-20 min, full function)
- Parallel testing
- Handler solution

Solution:
1) Dedicate memory tester
   - Memory Flash testers
   - Memory DRAM testers

2) SOC tester
   Is it possible to test 256M devices by using SOC tester?
   Yes, but, cost is a issue.
     - test time
     - parallel testing & handler
     - throughput
SiP Memory Test Options

- **Two-insertion, Two-platforms**
  - For Large Memory/Long Memory Test Time
  - Separate SOC and Memory Testers, Separate Insertions

- **Two-insertion, One-platform**
  - For moderate Memory Size/Test Time
  - Both SOC and Memory Tested on SOC Tester (with Limited Memory Test Capability or MTO), Two Separate Insertions

- **One-insertion, One-platform**
  - For Very Small Memory Size/Test Time
  - Both SOC and Memory Tested on SOC Tester Together in One Insertion
Case Study: Test Strategy for Memory in SiP

- Separate insertion Memory only on SOC tester with high site count
- Single insertion Memory & SOC tests
- 2nd insertion dedicated memory tester? If test times are multiple minutes
- SIP Manufactures will reduce Memory test times by eliminating Non failing patterns

❗ Test time in SIPs may be long on memories initially, but must/will be reduced over time.
Case Study Summary

• Memory Test Time Dictates Product Test Flow / Test Platform Choice

• High Volume, Long Memory Test time, Use Two Insertions, Memory Tester + SOC Tester for Cost Effective Test

• Low to Medium Volume, Use Dual Insertion on SOC Tester

• Long Memory Test Time Using Single Insertion on SOC Tester Is Cost Prohibitive

• Test Cost, Yield and Failure Analysis Are The Major Concerns

• DFT for Mixed-Signal and Memory Silicon is The Prefer Solution
SiPs ARE UNLIMITED

- Technology is not the limiting factor, and so future test requirements are hard to predict
- Especially true because technology (die) is coming from many suppliers
- And, what combinations will be integrated. Could be BB+RF, BB+MS, BB+MS+Memory, or all, or ??? (what will the next mobile application require?)
IS THERE A TEST SOLUTION?

• Overkill solution: buy test capacity that is a superset of all possible requirements
  > Does such a tester even exist today? For all of tomorrow’s future requirements?
  > Test cost with such platform will be inhibiting
  > Dual platform solution base on memory test time?

• Standardized test interface: Provide a standardized interface ala JTAG port
  > Provide sufficient test coverage and debug capability?
  > Can we standardize?
  > Nokia will want what Nokia wants

• None of these seem to be sufficient because they require knowing what the future holds, but cannot just look at the ITRS roadmap.
  > Who has been able to predict trends in the consumer market?
The Next Wave

Technology
Collaborative SiP Co-Design
For System Integration
Design for the End Product
IC, Package, System Integration
Collaborative Co-Design

- Architectural improvements required in Silicon process & design
- System integration issues will dominate SiP package technology

Silicon → Packages → Heat Sinks → Systems → Facilities
The next Step to SiP is System Integration:
Co-Design Technical Issues

Chip
Low-k

Digital / Analog / Mixed;
Peripheral/Matrix I/O

Integrated Electrical /
Thermal / Stress
Performance with Optimal
Package Solution

System Functional
Blocks With Optimal
Power Distribution,
Ground Isolation,
Thermal & Reliability
Collaboration Model

- IC Design
- Fab
- Packaging
- Test

* Design for Manufacturing
Out of the Box Thinking

Mindset & Cultural Change

• **Breakdown of walls**
  » Collaborate across supply chain
  » Co-Design – circuit, package, test, and system engineers
  » DFT: reduce test cost and cost of ownership

• **Readiness to integrate**
  » Integrate diverse technologies to provide greater functions for the consumers

• **Business Models**
  » Cooperation across supply chain & end user
  » Create Virtual IDM to achieve optimal efficiency
The End

Thank You