

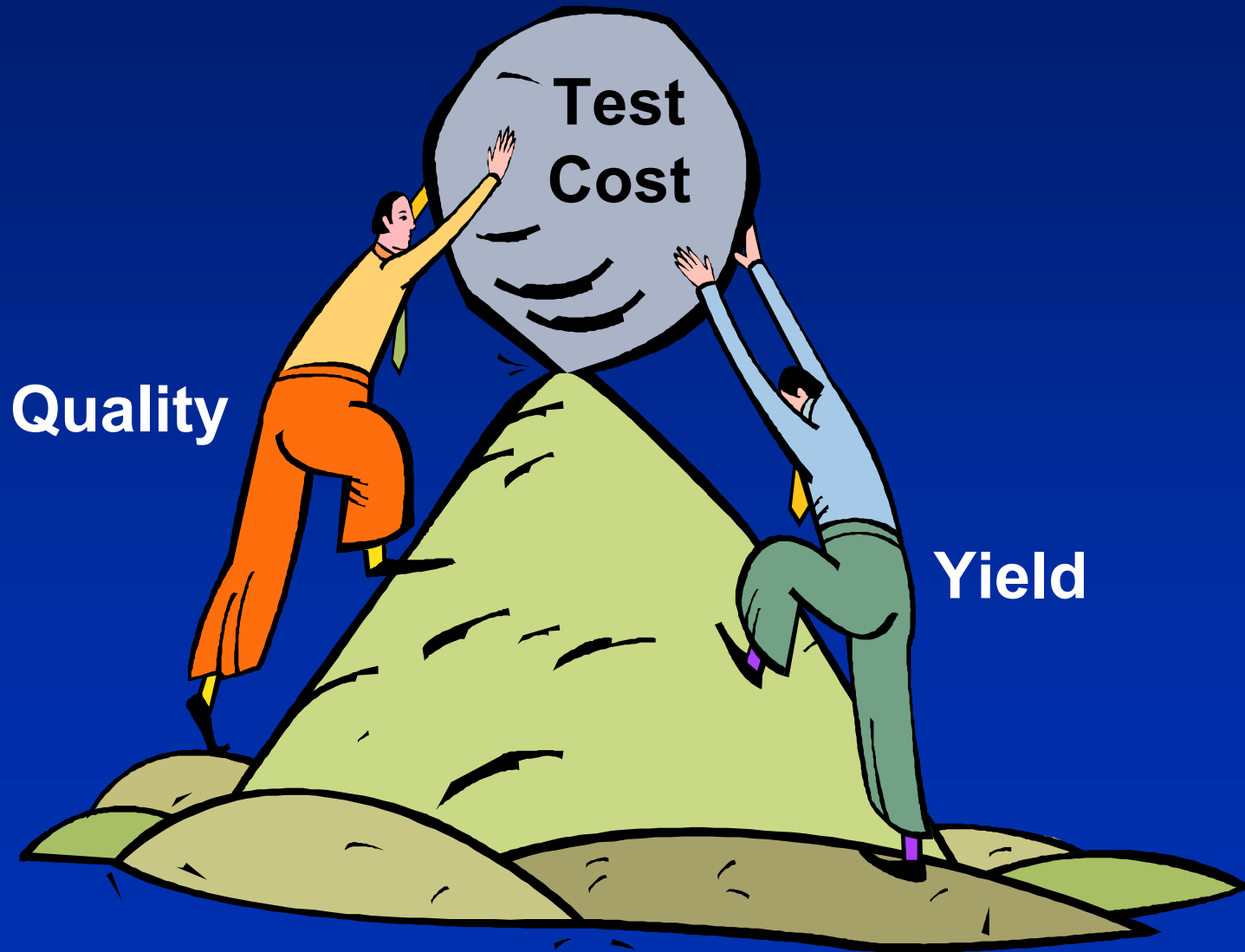
Some* DFT Challenges

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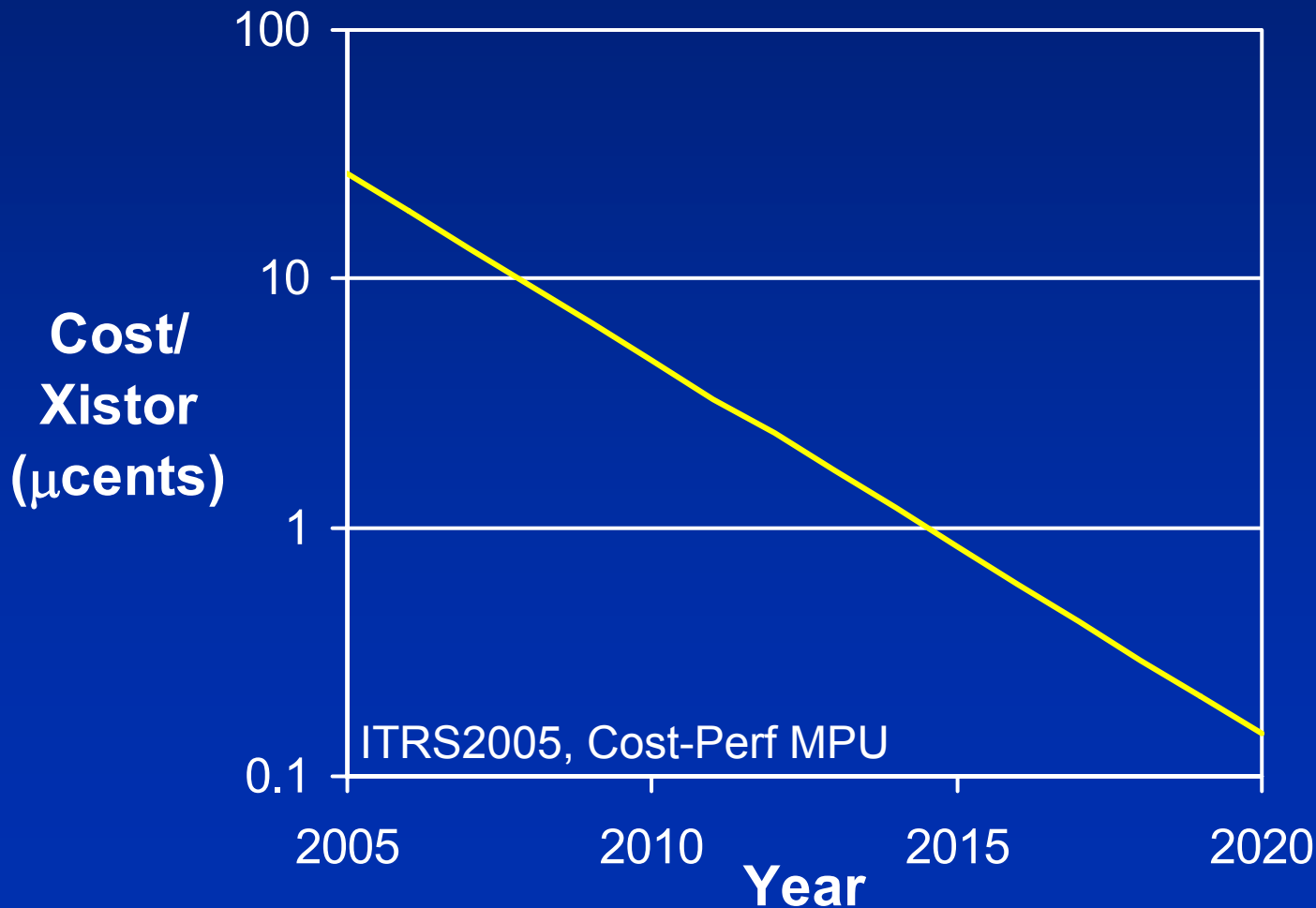
*The keynote is only 30 minutes

Life as a DFT Engineer



Test Cost Must Fall Fast

- Test cost/transistor must follow Moore's Law



**Need 100x
transistor
test cost
reduction!**

But ...

- Test cell cost not following Moore's Law
 - Already using DFT tester or old ATE
 - Handler and probe card cost not scaling
 - High-speed I/Os cost more

⇒ ***Must reduce test time***

- Parallel testing running out of gas

⇒ ***Must reduce test time per transistor***

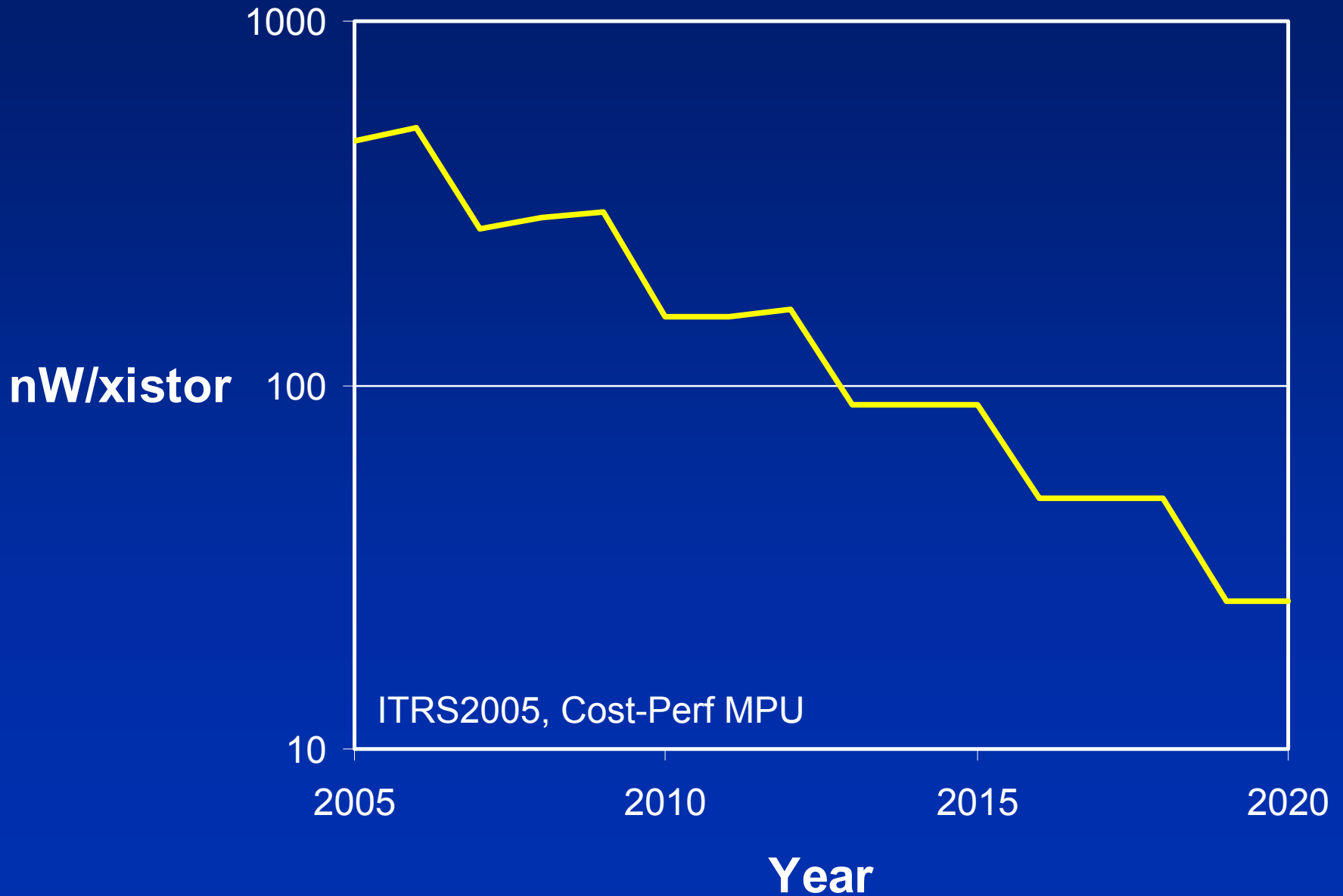
Reducing Test Time Per Transistor

- I/O Test
 - DC/AC test time must scale - DFT
- Mixed Signal
 - Apparently there's no silver bullet
- Memory
 - BIST – on-chip parallelism
- Logic
 - Tests/transistor rising to cope with variability, defects
 - Must wiggle more wires in less time

⇒ ***Higher power dissipation***



But ... Max Power/Transistor is Falling

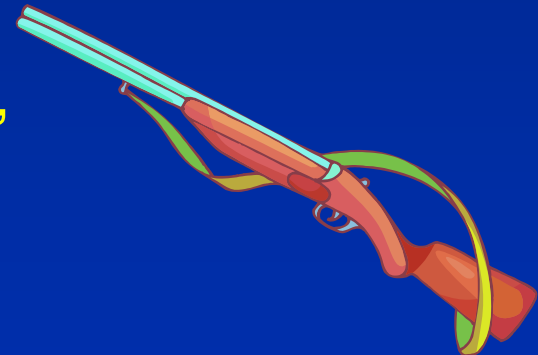


Future Digital Test All About Power?

- Fraction of chip that can be fired up at one time is decreasing
 - Mission-mode power constraints
 - Test supply noise
 - Test thermal limits
 - Limits intra-die test parallelism
- How to screen most defects per Watt?
 - Or is it defects per Joule?

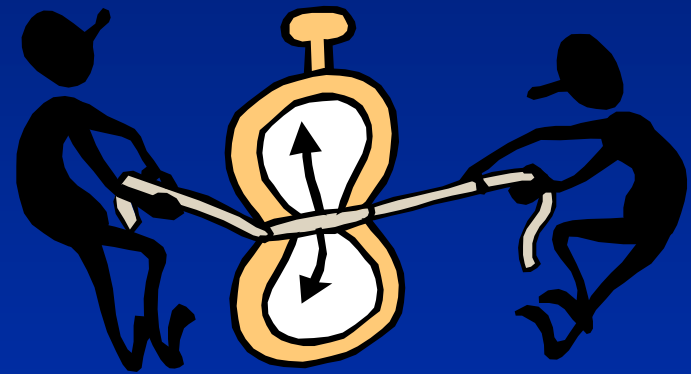
Eliminate Wasted Power/Energy

- Useless transitions
 - Scan power
 - Unnecessary capture power
 - Much research/commercial activity
- Low-odds test patterns
 - Luck – tails of BIST, WRP
 - Shotgun blasts – N-detect, DOR, ...
TARO, ...

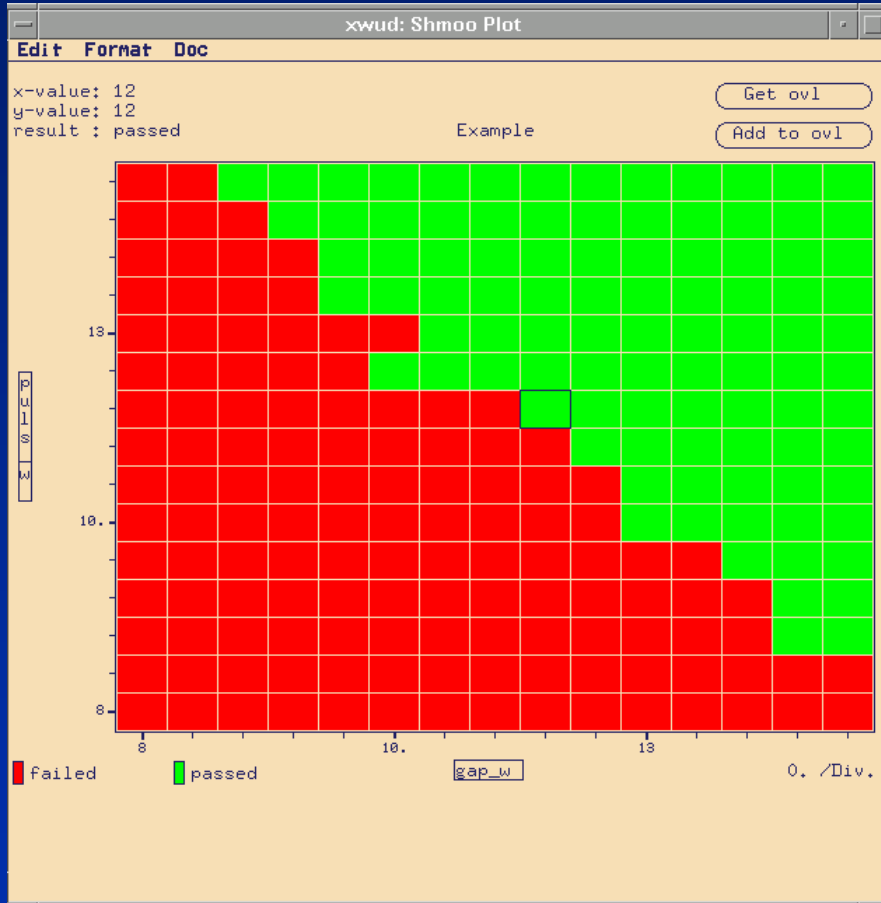


Squeeze Chip Harder Instead

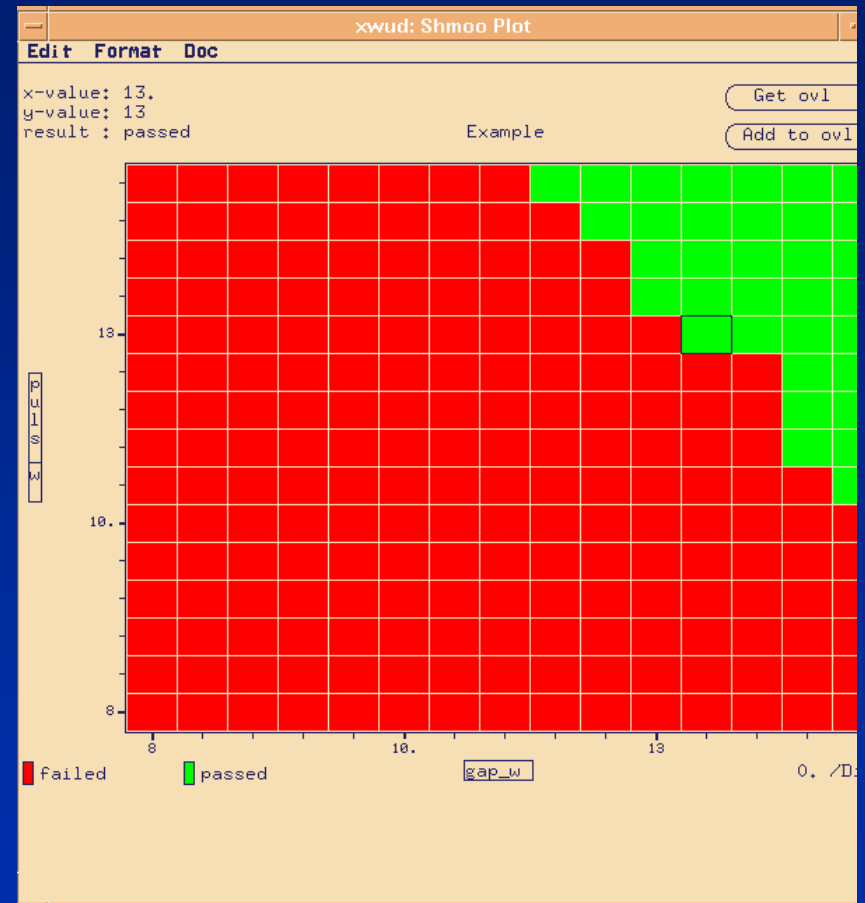
- IDDQ
- MINVDD
- KLPG
- TrueTime
- FineDelay
- Small Delay Defect
- Etc.



KLPG Squeezing

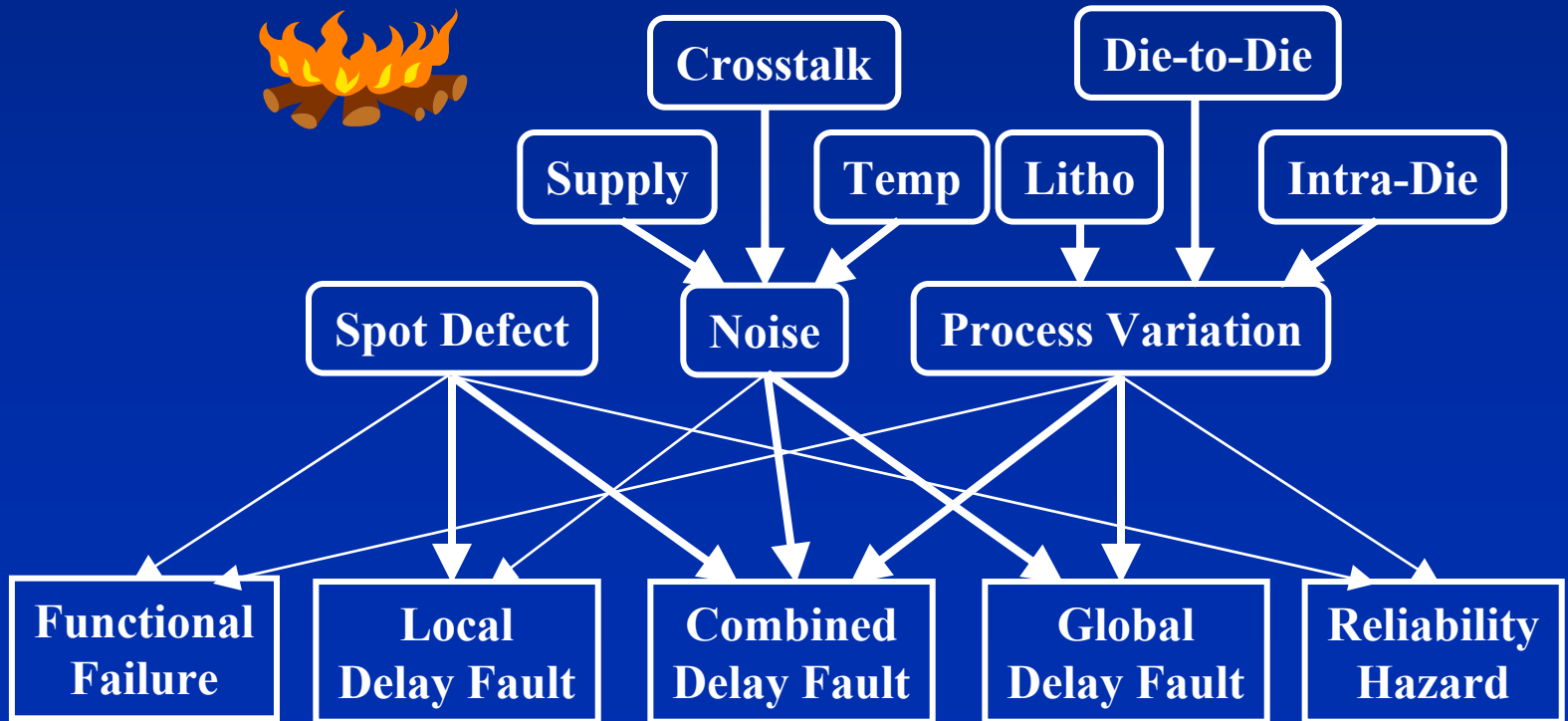
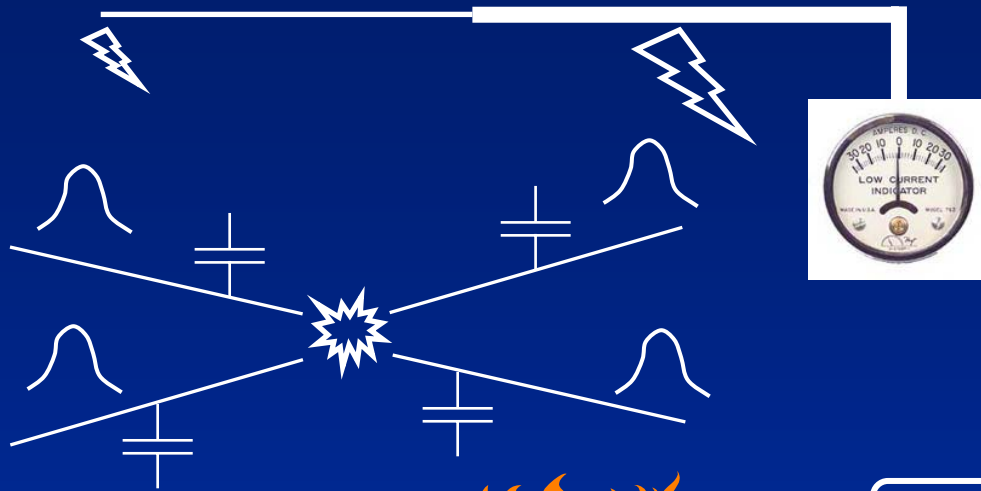


Transition Fault



KLPG

Target Only What Fails?



Kitchen Sink Fault Model

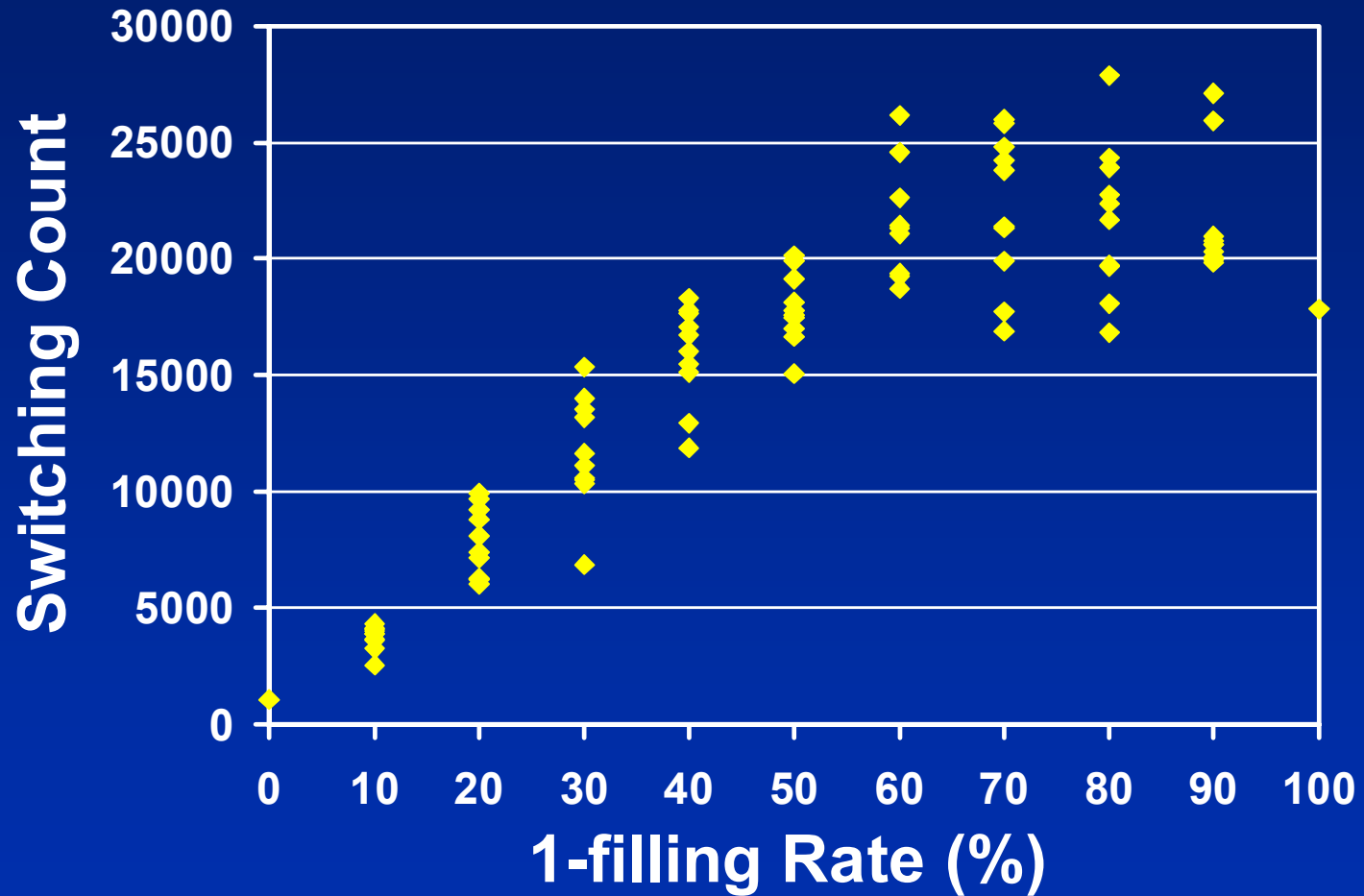
- How to minimize pattern count?
 - Fault tuples?
 - Compression?
- Link to DPM
 - Qiu/Walker, SDQM not the answer
 - Little characterization data
 - Use for sensitivity analysis instead
 - Example: if all paths through a line are short, pick any one



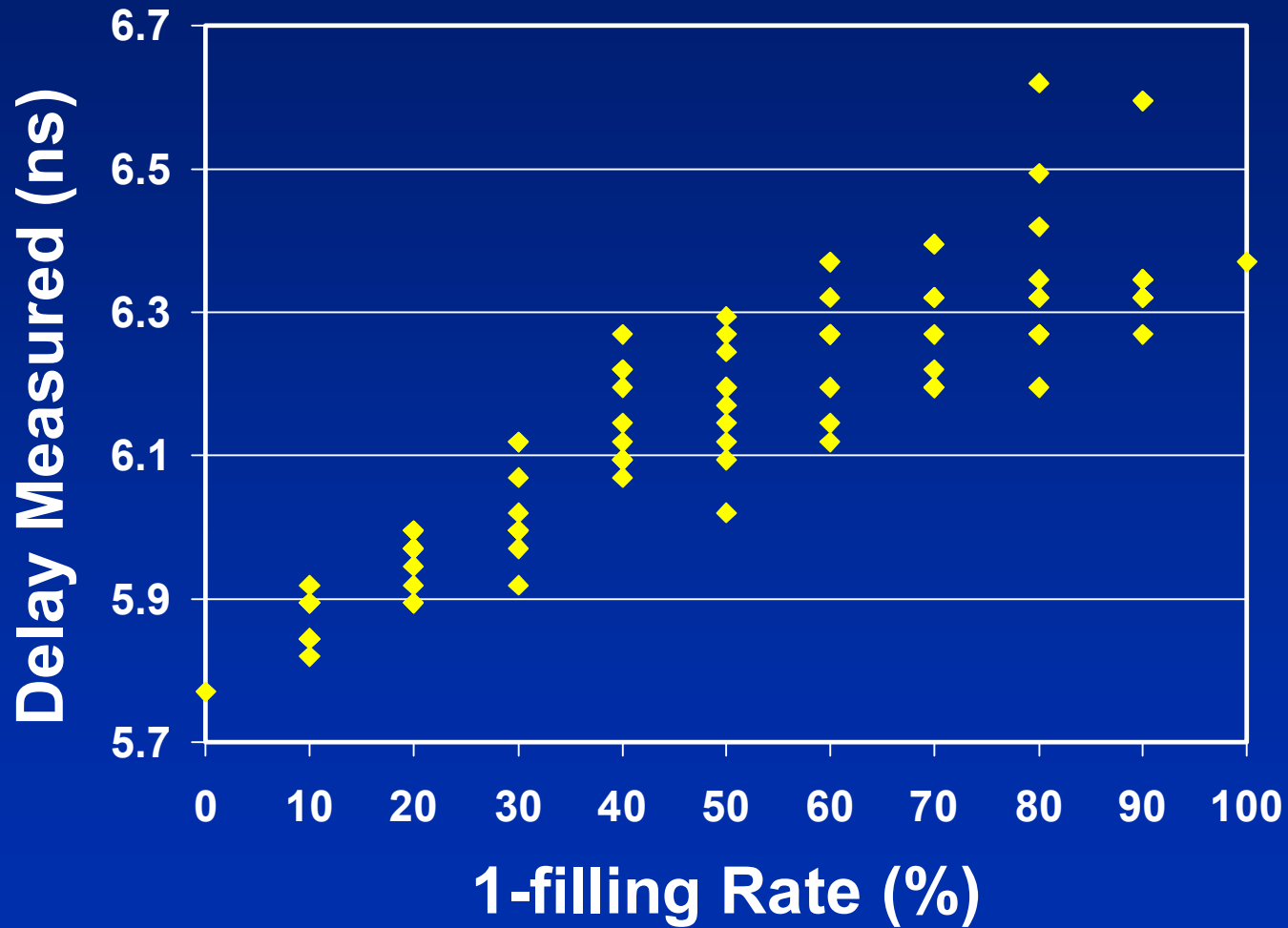
Scan DFT and Compression

- DFT that reduces pattern count may not help if it increases test power
 - Multiple scan enables
 - How it is used, more than the DFT itself
- Compression
 - Must avoid random fill of don't cares
 - Too much power
 - Lose some fortuitous detections

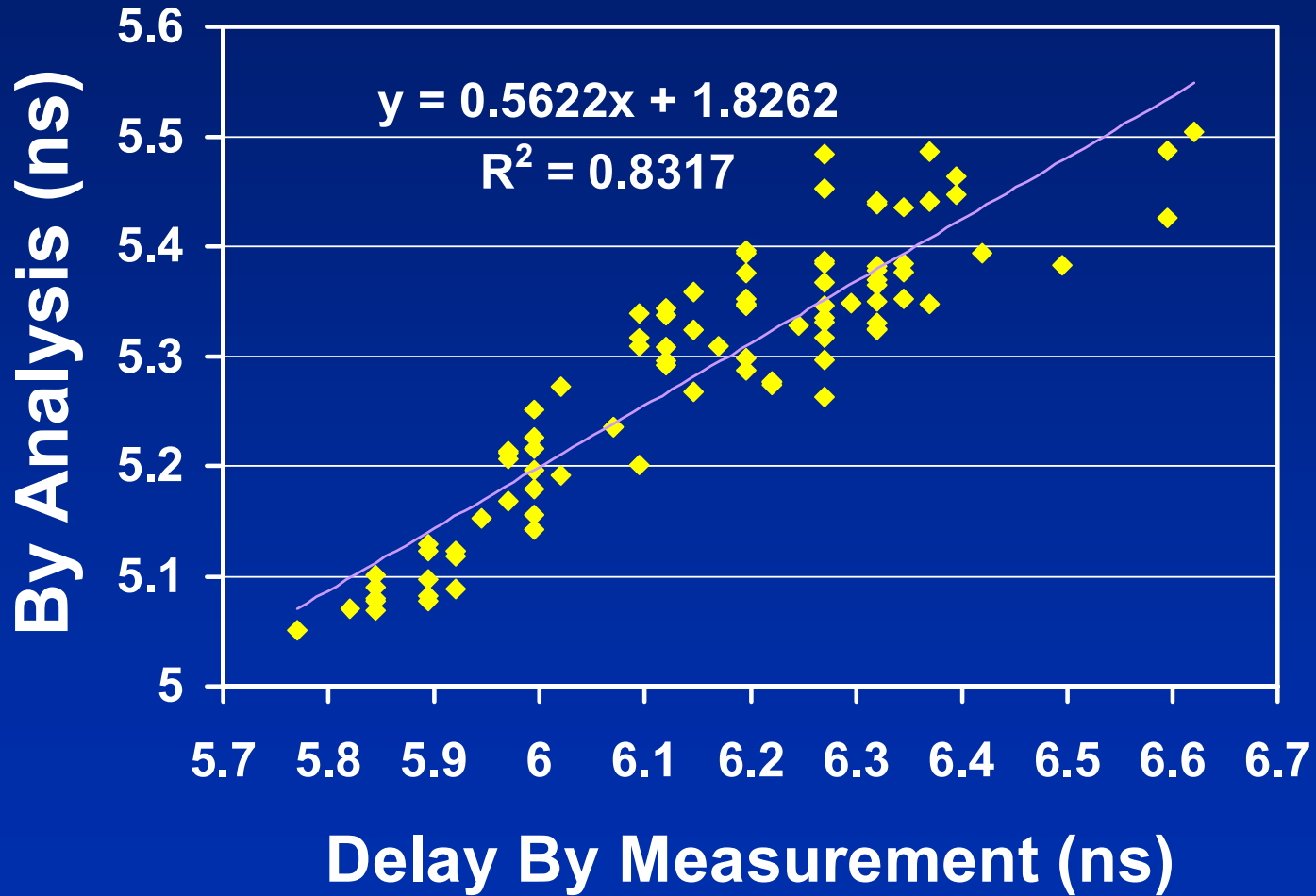
Filling Can Increase Capture Power ...



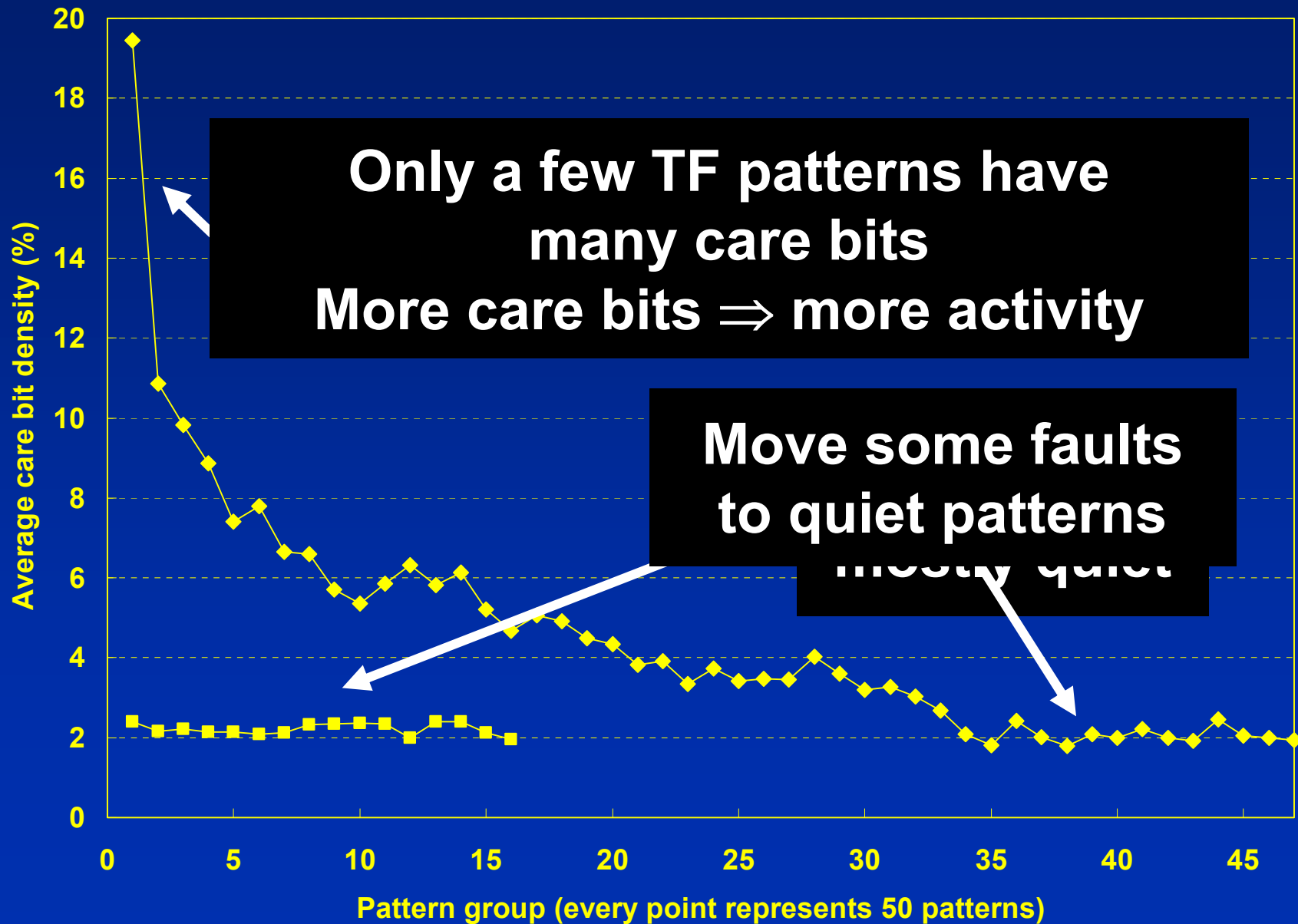
... Which Increases Circuit Delay



We Can Predict It ...



... And Fix It



DFT to Physical Design Linkage

- Test now requires full knowledge of physical design
- Past: scan chain routing
- Future: placement, power grid for supply noise, thermal control
- Maybe future: deterministic/litho process variations
- Not the future: defect characteristics (Qiu/Walker, SDQM) – little data

Final Thought: What About SOCs?

- How to deliver IP test knowledge to SOC designer?
- IPs cannot hide everything inside
 - Example: supply noise in wire-bond chip
- Affects SOC test schedule
- Need to abstract out-of-IP electrical/thermal behavior